UNIVERSITY OF ALBERTA

COMBINED FRAMING AND FEC CODING FOR DIGITAL MULTIPLEXED SIGNALS

BY

MAN YAU CHEUNG ©

A THESIS
SUBMITTED TO THE FACULTY OF GRADUATE STUDIES AND RESEARCH
IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF
MASTER OF SCIENCE.

DEPARTMENT OF ELECTRICAL ENGINEERING

EDMONTON , ALBERTA
CANADA
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ISBN 0-315-69986-8

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NAME OF AUTHOR : **MAN YAU CHEUNG**

TITLE OF THESIS : **COMBINED FRAMING AND FEC CODING FOR DIGITAL MULTIPLEXED SIGNALS**

DEGREE : **MASTER OF SCIENCE**

YEAR THIS DEGREE GRANTED : **FALL 1991**

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The undersigned certify that they have read, and recommend to the Faculty of Graduate Studies and Research for acceptance, a thesis entitled **COMBINED FRAMING AND FEC CODING FOR DIGITAL MULTIPLEXED SIGNALS** submitted by **Man Yau Cheung** in partial fulfillment of the requirements for the degree of **Master of Science**.

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ABSTRACT

Recent study has shown that the implementation of forward error control (FEC) codes in digital multiplexed signals can provide significant BER performance benefits (including error rate floor removal). This has motivated us to investigate the issues involved in implementing FEC codes in the DS3 and DS1 signal formats. As both of these signal formats have no spare allocations to accommodate the redundancy required by an FEC code, to implement FEC codes, some of their housekeeping bits must be freed up and reused in the FEC coding process.

It has been shown that the information contained in syndromes obtained in the decoding of FEC codes is sufficient for both the function of framing and error control. For this reason, the F-bits (primary framing bits) of the signals can be replaced by FEC parity check bits, and these check bits (reused bits) then provide the information required in frame finding and error control.

Because the F-bits in the DS3 and DS1 formats are both distributed over the frame, FEC codes used also have their parity check bits arranged likewise. New (novel) continuously compensated syndrome computation algorithms have been designed for both cases to produce a syndrome associated with every newly received bit, to facilitate accelerated frame finding.

Complete reframing and out-of-frame detection methods are developed. The resulting framing performance is analyzed and simulated to allow the selection of optimal reframing and out-of-frame detection criteria. The results show that the out-of-frame detection (OFD) performance is not as good as that of conventional framing. To overcome this problem, two new improved OFD schemes are developed for the DS3 format. The resulting overall framing performance is superior to that of conventional framing method. The BER performance gain of the proposed scheme is also analyzed for the DS3 case and

it is found that the output BER is reduced to 1360 P_e^2 if the channel errors are idependent. To determine whether the same level of BER gain would have been achieved in a real DS3 circuit, the error control rules inherent in the FEC code are used to analyze an error-event log of a commercial DS3 circuit. It is found the same order of magnitude BER improvement can be expected.

ACKNOWLEDGEMENTS

I would like to express my sincere thanks to my supervisors, Dr. W. A. Krzymien and Dr. W. D. Grover for their assistance, advice, and encouragement during the work on this project. Specifically, I would also like to thank Dr. W. D. Grover for proposing the initial idea of the project.

I would like to thank my supervisors and other members of the examining committee, Dr. K. Stromsmoe and Dr. A. E. Kamal, for taking time to read my thesis and to suggest improvements.

I am grateful to the staff and students of the Telecommunications Research Laboratories (TR Labs, formerly Alberta Telecommunications Research Centre) for providing a supportive and stimulating environment to carry out this work.

For financial assistance, I am deeply indebted to TR Labs and the University of Alberta for providing me with the Graduate Telecommunications Research Scholarship.

Finally, I would like to thank my family and friends, for their support and encouragement throughout the completion of this project.

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LIST OF ACRONYMS AND SYMBOLS

BER -	bit error rate
c -	is the confirmation count in the "c-successive-count" scheme
CCSC -	continuously compensated syndrome computation
check-sum -	a binary digit denoting whether an overall parity checksum is even or otherwise. check-sum = 0 indicates that the overall checksum is even
δ -	$= 1/n$, is the normalized duration of a single bit interval
d -	magnitude of shift (or slippage)
DED -	double error detection
DS1 -	Digital Signal level 1
DS1-FEC -	the (2316,2304) FEC code selected for the DS1 signal format
DS3 -	Digital Signal level 3
DS3-FEC -	the (1360,1348) FEC code selected for the DS3 signal format
ECU -	error correction unit
F-bit -	primary framing bit
FAB -	frame alignment bit
FEC -	forward error control
FF -	false in-frame
FIF -	the false in-frame state
FOTS -	fibre optic transmission system
g(x) -	the generator polynomial
HK-bits -	housekeeping bits of the DS1 or DS3 frames
INF -	the in-frame state
LSB -	the least significant bit
MF -	misframe
MF -	the misframe state
mod -	remainder of a modolo-2 polynomial division
MPX bits -	the masterframe overhead bits
MRF -	maximum (length) reframe

MSB -	the most significant bit
n_b -	number of DS3-FEC frames transmitted in one second
nC_k -	the number of combinations for choosing k out of n items
OFD -	out-of-frame detection
OOF -	the out-of-frame state
P_C -	probability of correct declaration of the in-frame state
p_d -	probability of successful detection of a valid FAB (in Chapter 2.) or a valid code word (in Chapter 3.)
P_F -	probability of false declaration of the in-frame state
PGF -	probability generating functions
p_m -	probability of mimic (probability of a block of bits obtained from a misaligned frame boundary mimicking a valid code word)
p_s -	probability of a random bit simulating the FAB pattern
R(x) -	the received word in the receiver buffer
S(x) -	the syndrome of the received word R(x)
SC OFD -	Shortened Code out-of-frame detection
SEC -	single error correcting
SEC-DED -	single error correcting and double error detection
SONET -	Synchronous Optical Network
synd -	a binary digit denoting whether a syndrome is zero or otherwise. synd = 1 indicates a non-zero syndrome has been obtained
$\tau(z)$ -	the signal transfer function of the reframe search process
T_{FF} -	average false in-frame time
T_{MF} -	average misframe time
T_{OF} -	average out-of-frame detection time
T_{RF} -	maximum average reframe time
u/d counter -	up/down counter
VLSI -	very large scale integration
x-o-o-K -	x-out-of-K criterion (x failures in the most recent K examined bits or words)

1. INTRODUCTION

Digital transmission networks make extensive use of the digital multiplexed signal formats [1]. A very low bit error rate (BER) for facilities carrying these signals is required by data applications which demand very high data integrity. Such low BER can possibly be achieved by employing facilities such as fibre optics. However, even with fibre optic systems, BER below a certain level cannot be achieved, because these systems exhibit the error floor phenomenon, i.e. the BER level cannot be further decreased by increasing the receiver input power. However, the BER level can be lowered by implementing a forward error control (FEC) code in the transmitted data. The implementation of an FEC code involves the transmission of additional parity check bits with the payload data. An example of such work is found in [2] where a highly efficient (224,216) single error correcting (SEC) FEC code was designed for each of the low-speed tributaries of a 565 Mbit/s lightwave system, resulting in the removal of error rate floors for the coded lightwave system. Another more efficient (6208,6195) single error correcting and double error detecting (SEC-DED) FEC code was suggested for implementation [3] in the STS-1 SONET signal, by placing FEC check bits in two unallocated bytes of this signal format. Both of these design involved the use of additional overhead (on top of the payload capacity) to accommodate the additional redundancy required by the FEC code.

Unfortunately, no spare capacity (overhead) is available in existing digital multiplexed signal formats to incorporate FEC codes. If an FEC code is to be implemented in the existing signal format without sacrificing the payload capacity or increasing transmission bit rate, some housekeeping bits must somehow be freed up and reused as FEC parity check bits. The housekeeping bits, such as the primary framing bits (F-bits, in the DS3 and DS1 signals [1], used for the function of framing) can provide the necessary redundancy required by the FEC code. However, if their function is changed, the function of framing that they normally provide must be implemented in an alternative way. The alternative approach to framing have been suggest by Frey[4], which uses the information obtained in the FEC decoding process to perform frame finding and out-of-frame detection. However, this approach has not been adopted in any of today's digital signal formats (standardized in the 1960's and 70's). This is probably due to the fact that the high speed VLSI circuits and numerous storage elements, required to implement efficient FEC codes in the digital signals, were either not available or too costly in the past. Recent availability of high speed VLSI technology at low cost has prompted us to consider the integration of the FEC and framing functions.

1.1 Framing

Digital signals of a lower bit rate are serially combined in a periodic manner (time-division multiplexed) into a higher bit rate signal for transmission (e.g. 7 DS2 signals are multiplexed to form 1 DS3 signal). Each cycle of the multiplexed signal which contains all the lower rate signals is called the frame. Data from each of the lower bit rate signals then forms the components (channels) of each frame in the resultant higher rate signal. To identify and recover the data of each channel at the receiver (i.e. to demultiplex the signal) a fixed pattern of frame alignment bits (FAB) is inserted in each frame (e.g. F-bits are used in the DS3 and DS1 signal formats) to mark the start (or finish) of the frame. By scanning for the periodic occurrences of these FAB's, the receiver can establish frame alignment before demultiplexing the signal.

1.2 Proposed Combined Framing and Forward Error Control (FEC) Scheme

It has been shown [4] that the redundancy contained in forward error control (FEC) coding can be used for both framing and error control at the receiver. This is because in the absence of errors, the code words presented to the FEC decoder are only detected as valid, when the decoder is synchronized to the correct word boundary. When the decoder is not synchronized, the decoded words are almost always (typically in at least

99.999% of all cases) detected as invalid. Therefore, in low BER systems (BER $\leq 10^{-6}$), the FEC decoder can be modified and used to scan through misaligned word (frame) boundary positions until the aligned position is obtained.

This concept is applied here to the DS3 and DS1 signal formats, where the primary framing bits are replaced by FEC parity check bits. The framing is then based on the observation of syndromes evaluated in the receiver. As the FAB's (F-bits) in the DS3 and DS1 signals are both distributed throughout the frame, the check bits of the suitably selected FEC codes are also arranged in the same way. The resulting FEC coded DS3 and DS1 carrier signals remain compatible with today's transport network. Applications include high performance private DS3 and DS1 networking where the BER advantage of FEC and the performance monitoring role of FEC [3] are both desirable.

However, the issues to be addressed when applying the combined framing and FEC concept to the DS3 and DS1 signal formats are:

i) framing performance of the new scheme versus that of conventional framing.

ii) resulting BER performance gain.

These are the main topics of this thesis.

It must be mentioned that while the combined framing and FEC coding concept introduced here is applicable to any digital multiplexed signals with low overheads, the emphasis of this thesis is on the application of the proposed concept to the DS3 signal format. The application to the DS1 signal format is included only as a second example. Because the analysis and derivation methods used for the two formats are identical, hence the details of the analysis and derivation steps are not discussed for the DS1 case.

1.3 Outline of the Thesis

Chapter 2 describes the analysis involved in the characterization of frame performance (in general). Specifically the performance of conventional DS3 (F-bit) framing is analyzed, and the results presented. Chapter 3 describes the issues involved in realizing the combined framing and FEC coding scheme for the DS3 signal format. These includes: (i) the selection of an FEC code for the DS3 signal format; (ii) the encoding and decoding schemes involved; (iii) the development of new every-bit-time syndrome computation techniques (for various code word formats, i.e. code words with different arrangements of check bit placement) which enables fast framing; (iv) the characterization of the framing parameter for FEC framing; v. the effective BER with the FEC protection for the DS3-FEC code, and the BER advantage of the FEC code for a commercial DS3 circuit is also analyzed based on an error-event data log obtained for the circuit. Chapter 4 describes two improved out-of-frame detection schemes which have better out-of-frame detection performances than those of the out-of-frame detection scheme presented in Chapter 3. Chapter 5 compares the framing performance of FEC framing, including those of the improved out-of-frame detection methods, with those of conventional DS3 framing. Chapter 6 describes an example of applying the combined framing and FEC coding concept to the DS1 signal format. The framing performances and BER advantage are analyzed and presented. Chapter 7 provides a summary of the work done in this thesis as well as conclusions and areas of possible future work.

2. CONVENTIONAL DS3 FRAMING

Before presenting the timing parameters which apply to the conventional DS3 framing, a brief description of the framing process and its parameters is given first.

2.1 Framing and Its Timing Parameters

The framing circuit's behaviour can be described by the finite state machine shown in Fig. 2.1. The four possible states are :

- INF (in-frame): The framing circuit is frame aligned and declares it.
- MF (mis-frame) : The framing circuit is frame aligned but declares the opposite.
- OOF (out-of-frame) : The framing circuit is frame misaligned and is trying to re-establish the in-frame state.
- FIF (false in-frame) : The framing circuit is frame misaligned but falsely declares alignment.

The four relevant transitions between these states are shown (by continuous lines) in Fig. 2.1. Their respective timing parameters are important in characterizing a given framing strategy. The other transitions (indicated by dashed lines) in practice almost never occur and therefore are not relevant.

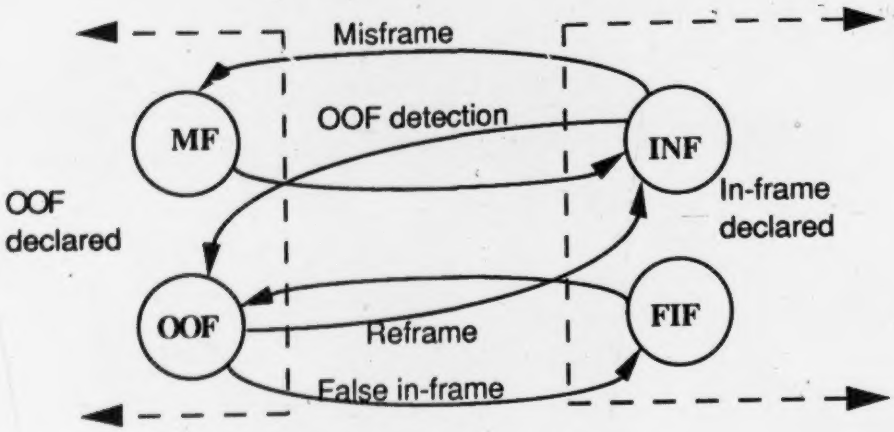


Fig. 2.1 State transitions in frame alignment process.

2.1.1 Reframing

Once the OOF state has been declared, the conventional framing circuit begins a search process by successively slipping to the next bit position (i.e. by generating bit "slips" in the frame alignment timing) in the frame and attempts to find a match with the FAB pattern. When a match is found, the current bit position (at which the match occurs) is treated as the candidate framing position, and the search process is temporarily suspended (and the current position is dwelled on). The candidate position is subjected to a confirmation process which checks whether the FAB pattern is repeated in the FAB positions of subsequent frames. The confirmation is used to eliminate the possibility of locking the framing circuit onto a misaligned position which contains the FAB pattern simulated (or mimicked) by transmitted data. When the position dwelled on due to a data simulated FAB pattern is rejected by the confirmation test, the search process resumes. When all non-aligned positions have been rejected (i.e. the falsehood detection process has been completed), and the framing circuit arrives at the true frame alignment position, a successful confirmation must occur before the in-frame state is declared. If an error corrupts the FAB during the confirmation interval, the unsuccessful confirmation forces another search starting from one bit after the true aligned position. These repeated search and confirmation tests continue until a final successful confirmation declares the in-frame state. A "c successive count" confirmation scheme is used for the normal reframing process in DS3 (and DS1). The value of c is chosen large enough so that false in-frame declarations are impossible or made extremely rare. Typical values of c are from 12 to 20.

2.1.2 Maximum Average Reframe Time(T_{RF})

Reframe time is the time it takes to re-establish the INF state from the OOF state. In the worst case, the framing circuit starts the reframing process just one bit after the true frame aligned position. This means the search and confirmation process has to reject the maximum possible number (less one) of positions in the frame before arriving at the aligned position. The average time for this maximum length reframe search is called the maximum average reframe time.

2.1.3 False in-Frame Time(T_{FF})

During the reframing phase, random data can mimic the FAB pattern. When multiple mimics occur successively at frame intervals more times than the confirmation threshold, c, the framing circuit will falsely declare the INF state. The average time to such a declaration is called the false in-frame time. Of course, if it is a false in-frame declaration during a reframe search, the OOF state is quickly redeclared and the search goes on after having lost some time due to the apparent halt condition.

2.1.4 Out-of-Frame(OOF) Detection

During the in-frame state, the framing circuit checks for the occurrences of the correct FAB's every FAB interval. If errors of the expected FAB's occur more times than a a confirmation threshold, the OOF state is declared. The confirmation process is used to reduce the probability of spurious OOF declaration caused by channel errors. The "c successive count" and the "x-out-of-K" (x failures in the most recent K tests) criteria are commonly used. The latter criterion is used in conventional DS3 (and DS1) system design practice.

Systems which use small values of x (or c) will have faster OOF detection times but are more prone to misframes caused by line errors. The value of x (or c) is chosen optimally for a relative fast OOF detection while achieving very long time between misframes even at degraded BER levels (such as 10^{-5}).

2.1.5 Out-of-Frame Detection Time(T_{OF})

The out-of-frame detection time is the average time it takes to detect an OOF condition after it has occurred. It is dependent on the value of x (or c). It is also dependent on how often random data at the misaligned position locked onto by the framing circuit simulate the FAB pattern. This is because the occurrence of a simulation causes the framing circuit to maintain its declaration of the in-frame state, hence delaying the OOF detection process.

2.1.6 Misframe Time(T_{MF})

Multiple corruptions of the FAB's by line errors during the in-frame state cause the framing circuit to incorrectly declare the OOF status. The average time to such a declaration is called the misframe time.

A good framing strategy has short T_{RF} and T_{OF} times, while achieving very long T_{FF} and T_{MF} times.

2.1.7 Factors Affecting Framing Performance

In general the framing performance of a given system is affected by the following factors:

i. choice of the in-frame and the OOF detection confirmation threshold values (c in the c-successive-count criterion, or x and K in the x-out-of-K criterion) .

ii. the BER level in the system - this determines how often the FAB's are corrupted, or conversely, how often the FAB's are successfully detected.

iii. the number of successive frame alignment bit positions simultaneously examined by the framing circuit during the reframing search process, as this determines how likely the examined FAB pattern is simulated.

The probability for a correct recognition (successful detection) of a valid FAB pattern is denoted as p_d and the probability of a random bit simulating the FAB pattern is denoted as p_s. Higher values of p_d are more desirable as they bring shorter reframe times and longer misframe times. Lower values of p_s are more desirable as they bring shorter OOF detection times, longer false in-frame times, and shorter reframe times (because this results in fewer, on average, simulations of the FAB's, hence allowing a faster search process).

In the case of conventional DS3 framing, only one FAB (or F-bit) is examined by the framing circuit at a time. Therefore the probability of a successful detection, p_d, of the F-bit is equal to $(1-BER_{channel})$ and the probability of simulation, p_s, of the F-bit is equal to 1/2.

2.2 DS3 Masterframe Structure

The DS3 signal consists of masterframes, the structure of the masterframe format is shown as follows:

$\mathbf{M_0}$ [84] $\mathbf{F_1}$ [84] $\mathbf{C_{11}}$ [84] $\mathbf{F_0}$ [84] $\mathbf{C_{12}}$ [84] $\mathbf{F_0}$ [84] $\mathbf{C_{13}}$ [84] $\mathbf{F_1}$ [84]
$\mathbf{M_1}$ [84] $\mathbf{F_1}$ [84] $\mathbf{C_{21}}$ [84] $\mathbf{F_0}$ [84] $\mathbf{C_{22}}$ [84] $\mathbf{F_0}$ [84] $\mathbf{C_{23}}$ [84] $\mathbf{F_1}$ [84]
$\mathbf{M_0}$ [84] $\mathbf{F_1}$ [84] $\mathbf{C_{31}}$ [84] $\mathbf{F_0}$ [84] $\mathbf{C_{32}}$ [84] $\mathbf{F_0}$ [84] $\mathbf{C_{33}}$ [84] $\mathbf{F_1}$ [84]
P [84] $\mathbf{F_1}$ [84] $\mathbf{C_{41}}$ [84] $\mathbf{F_0}$ [84] $\mathbf{C_{42}}$ [84] $\mathbf{F_0}$ [84] $\mathbf{C_{43}}$ [84] $\mathbf{F_1}$ [84]
P [84] $\mathbf{F_1}$ [84] $\mathbf{C_{51}}$ [84] $\mathbf{F_0}$ [84] $\mathbf{C_{52}}$ [84] $\mathbf{F_0}$ [84] $\mathbf{C_{53}}$ [84] $\mathbf{F_1}$ [84]
X [84] $\mathbf{F_1}$ [84] $\mathbf{C_{61}}$ [84] $\mathbf{F_0}$ [84] $\mathbf{C_{62}}$ [84] $\mathbf{F_0}$ [84] $\mathbf{C_{63}}$ [84] $\mathbf{F_1}$ [84]
X [84] $\mathbf{F_1}$ [84] $\mathbf{C_{71}}$ [84] $\mathbf{F_0}$ [84] $\mathbf{C_{72}}$ [84] $\mathbf{F_0}$ [84] $\mathbf{C_{73}}$ [84] $\mathbf{F_1}$ [84]

Fig. 2.2 The DS3 signal format.

The **bold** characters are the 'housekeeping' (HK) bits which separate groups of 84 tributary payload bits, denoted by [84]. The payload bits are a multiplex of 7 plesiochronous DS2 tributaries using a pulse-stuffing synchronization technique [5] . Each DS2 is transmitted at 6.312 Mb/s ±30 ppm. The $\mathbf{F_1}$ and $\mathbf{F_0}$ bits are the primary frame-alignment bits (the F-bits). They have a fixed periodic 1-0-0-1 pattern for which the framing circuits hunts, to establish frame alignment of the basic DS3 frame. After the alignment of the DS3 frame, the arrangement of individual frames into a masterframe is required so as to facilitate the identification of the tributary to which each set of three stuff-control C-bits pertain. Masterframe alignment is found by decoding the M_0-M_1-M_0-P-P-X-X pattern. M_0 and M_1, (M-bits), are fixed 1 and 0 values. P is the parity over the preceding masterframe and X is a signalling bit reserved for customer use and is random. P-P and X-X denotes their duplication.

$\mathbf{C_{i1}}$-$\mathbf{C_{i2}}$-$\mathbf{C_{i3}}$ are used to indicate the presence of a *stuffed pulse* in frame **i**. Pulse stuffing synchronization [6] is the technique used to accommodate asynchronism in the input tributaries. Note the actual rate per tributary in the DS3 frame is 6.3157 Mb/s, and the inputs are at 6.312 Mb/s ±30 ppm. The difference frequency is compensated by transmitting 'stuff' bits as required for each tributary and indicating the presence of the stuffed bits to the demultiplexer via the C-bits. The presence or otherwise of a stuff bit in the ith tributary is indicated by $\mathbf{C_{i1}=C_{i2}=C_{i3}} = 1$ or $\mathbf{C_{i1}=C_{i2}=C_{i3}} = 0$ respectively. C-bits are triplicated and they are decoded at the demultiplexer using majority logic-detection. This arrangement provide single error protection for the C-bits.

2.3 Estimation of Timing Parameters

2.3.1 Probability Generating Functions (PGF).

The probability generating function of the state transition time X between two states in a finite state machine is defined as follows:

$$P_X(z) = E[z^X] = \sum_i p_i z^{x_i} = p_0 z^{x_0} + p_1 z^{x_1} + p_2 z^{x_2} + \dots \qquad (2.1)$$

where E[ ] denotes the expectation operator, z is a dummy variable, and p_i are the discrete probabilities for X being x_i, for i = 0, 1, 2, ... The mean and variance of X can be obtained using the following properties of the PGF:

$$E[X] = P'_X(1) \text{ and,}$$

$$VAR[X] = P''_X(1) + P'_X(1) - \{P'_X(1)\}^2 \qquad (2.2)$$

The four timing parameters for conventional framing are estimated using probability generation functions derived as signal transfer functions in the generalized state transition diagram of Sittler [7] and Choy [8]. The generalized state transition diagrams depict the state transitions by marking each transition branch with a transitional probability and the transition time (whereas branches of a conventional state transition diagram only have the transition probabilities). Each transition time is expressed as an exponent of the z variable (e.g. z^2 means that a time of two units is required to complete the associated transition). The PGF of the transition time of interest between two specified states is simply the signal transfer function of the state transitions. The signal transfer function can be easily obtained using commonly known signal flow graph reduction methods [9].

2.3.2 Maximum Reframe (MRF) Times

The specified value of the maximum average reframe time for the DS3 signal is 2msec [1]. To meet this specification one implementation described in [10] uses a sequential search process that is capable of performing continuous slips during the search process.

i. Search process

The falsehood detection process for a maximum length search requires the rejection of all but one (n-1) bits of the frame. The rejection of one bit (i.e. the framing circuit timing shifts from one bit position to the next bit position) is depicted as the transition from state "i" to "i + 1" in Fig. 2.3. If the first examined bit associated with bit position i (state i) violates the F-bit pattern, a transition is made to state i+1 (the next bit position), this transition requires one slip (and for a sequential search process each slip takes one F-bit interval plus one bit or 1+δ time). However, if the first examined bit simulates the F-bit pattern, state i is maintained for at least an additional F-bit interval (1 unit time) until the examined bit violates the F-bit pattern. The model in Fig. 2.3. assumes that the confirmation threshold c is infinite when performing the falsehood detection process, i.e. a non-aligned position is always rejected and it can never be accepted (declared) as the in-frame position (false in-frame). This assumption incurs negligible discrepancy in the estimated values because c is often chosen large enough to ensure that a false in-frame practically never happens.

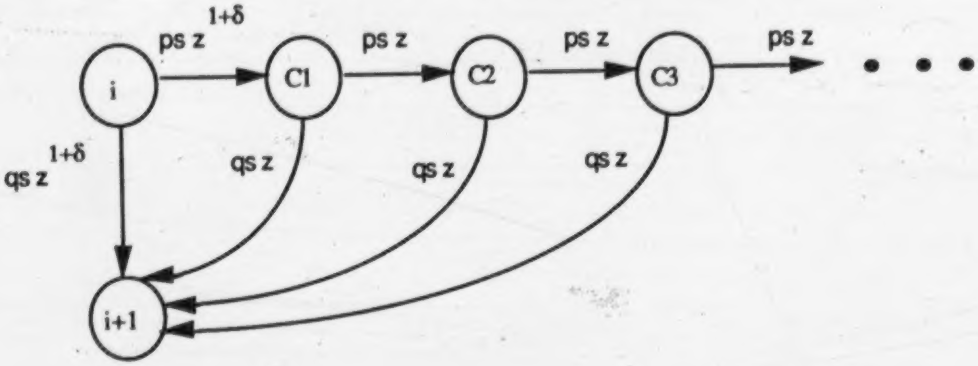


Fig. 2.3. Falsehood detection process for 1 bit.

Reduction of the flow graph in Fig. 2.3, yields the overall state transition transfer function from the state i to i+1:

$$\frac{q_s\, z^{1+\delta}}{1 - p_s\, z} \tag{2.3}$$

For the maximum length search (n-1) bits must be rejected and it takes a final (1+δ) time to slip to the true in-frame position. Therefore the search process has the signal transfer function:

$$\tau(z) = \left(\frac{q_s\, z^{1+\delta}}{1 - p_s\, z}\right)^{n-1} z^{1+\delta} \tag{2.4}$$

where $p_s = 1/2$ is the probability of transmitted data simulating (or mimicking) a single FAB, and $q_s = 1 - p_s$. $\delta = 1/n = 1/170$ is the normalized (in reference to one quarter frame) duration of a single framing bit interval in the DS3 frame.

ii. Combined search and confirmation

The search and confirmation (reframe) process is depicted in Fig. 2.4. After completing the maximum length search (its timing is characterized by τ(z)), the framing circuit arrives at the true frame alignment position. At that point, if the F-bit is not corrupted (or a successful detection of the F-bit) a count of 1 is registered, otherwise the confirmation count remains at zero and a repeat maximum length search is required. To complete the confirmation c such successful detections are required and any unsuccessful detection (or F-bit error) would reset the confirmation count back to zero. The signal transfer function of the reframe process is:

$$P_{RF}(z) = \frac{p_d^c\, \tau(z)\, z^{c-1}}{1 - q_d\ \tau(z)\dfrac{1 - p_d^c\ z^c}{1 - p_d\, z}} \tag{2.5}$$

where p_d is the probability of correct detection of a single true frame alignment bit (FAB). Hence $q_d = 1 - p_d$ is the bit-error-rate (BER) in the transmission channel. The function $\tau(z)$ is given by (2.4)

The value of c is typically equal to 20.

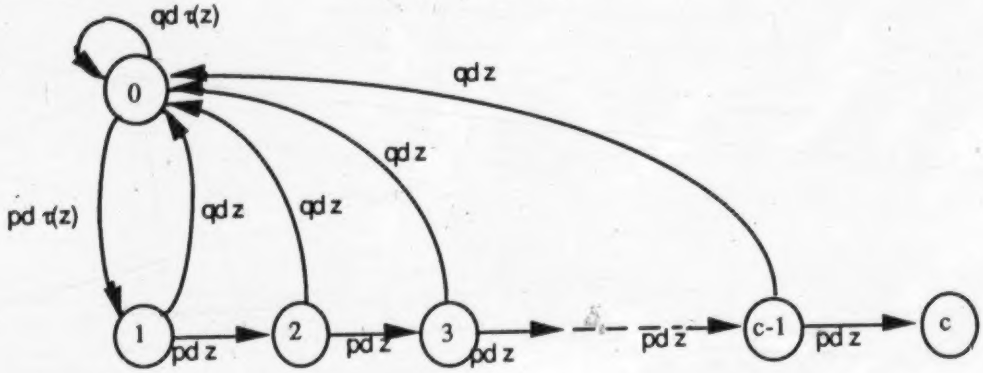

qd τ(z)
qd z
qd z
pd τ(z)
qd z
qd z
0
1
2
3
c-1
c
pd z
pd z
pd z
pd z
pd z

Fig. 2.4 Reframe declarations procedure

2.3.3 False in-frame (FF) Times

The false in-frame state transition diagram is shown in Fig. 2.5. Once the OOF state is declared, the reframing procedure starts the search by continuously slipping to the next bit position every (1+ δ) time, while the examined bits do not simulate the F-bit pattern. When an F-bit simulation (with a probability p_s) occurs, the confirmation process is started. Consequently, c successive simulations cause a false in-frame declaration.

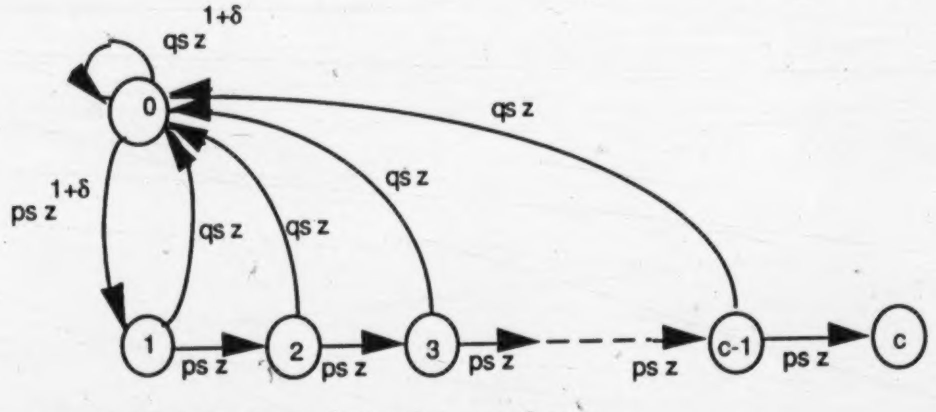

1+δ
qs z
qs z
qs z
1+δ
ps z
qs z
qs z
0
1
2
3
c-1
c
ps z
ps z
ps z
ps z
ps z

Fig. 2.5 False-in-frame declaration procedure.

The signal transfer function for the false in-frame process is:

$$P_{FF}(z) = \frac{p_s^c \, z^{c+\delta}}{1 - q_s \; z^{1+\delta} - p_s \, q_s \, z^{2+\delta} \dfrac{1 - (p_s \, z)^{c-1}}{1 - p_s z}} \tag{2.6}$$

2.3.4 Probability of Correct Declaration (P_C) of the In-Frame State

The declaration of the in-frame state as a result of a reframe can either be a correct or incorrect. For a c-successive-count confirmation and a frame size of n, a correct alignment is obtained when a candidate position is in the true aligned position and c-successive successful detections have occurred. Its probability is given by:

$$\frac{p_d^c}{n} \tag{2.7}$$

An incorrect alignment is obtained when a candidate position is not the true aligned position but c-successive data simulated F-bits patterns have occurred. Its probability is given by:

$$\frac{n-1}{n} \, p_s^c \tag{2.8}$$

Therefore, the probability of a correct frame alignment when an in-frame state has been declared is:

$$P_C = \frac{p_d^c}{p_d^c + (n - 1) \; p_s^c} \tag{2.9}$$

And the probability of a false declaration is:

$$P_F = 1 - P_C \tag{2.10}$$

where p_d and p_s are the same as those specified in equation (2.1) and (2.2).

A good framing procedure should have a extremely small value of P_F.

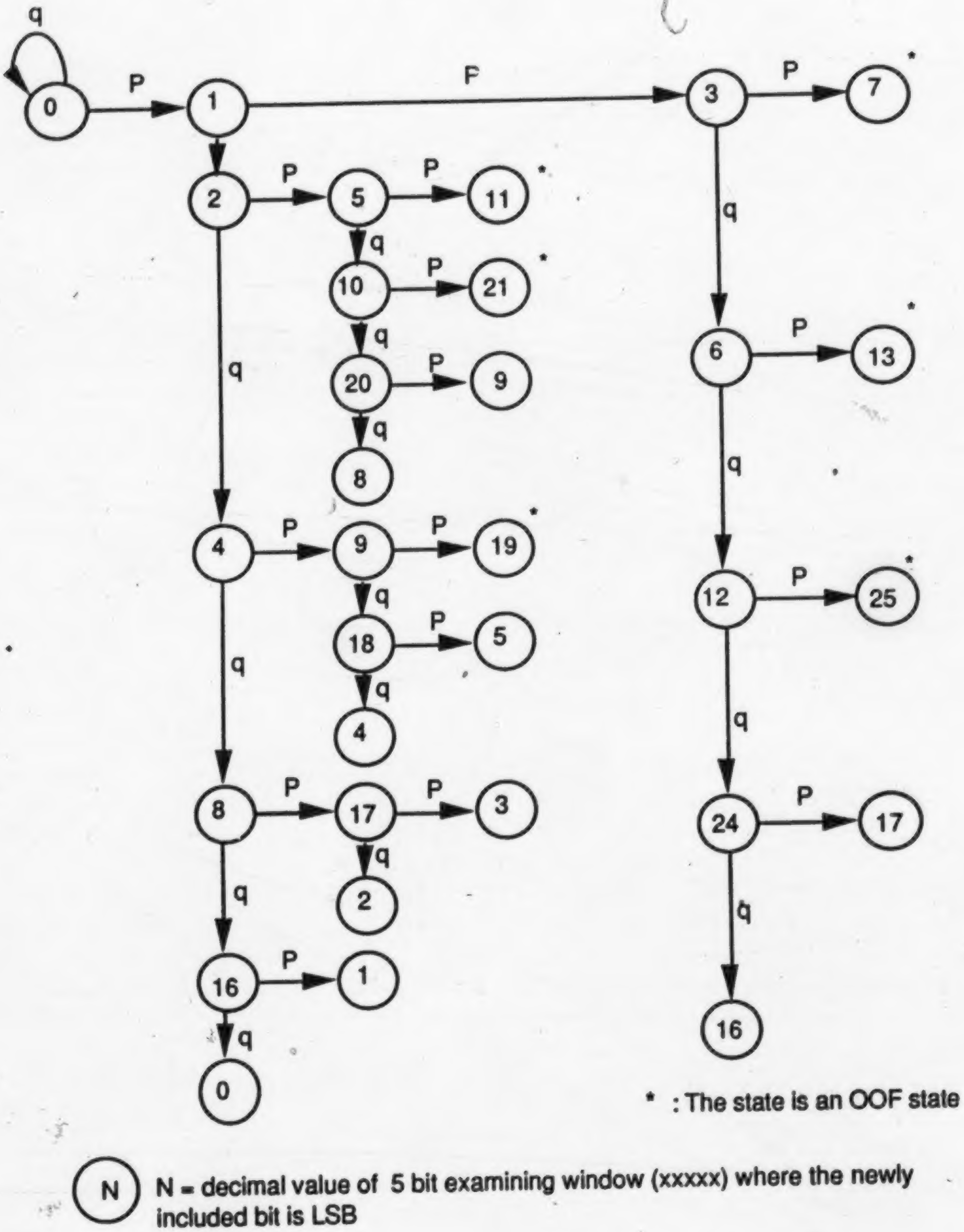
2.3.5 Out-of-frame (OFD) Detection and Misframe (MF) Times

The 3-out-of-5 and 4-out-of-7 OOF detection criteria are recommended in [1] for the DS3 signals. In the x-out-of-K (x-o-o-K) OOF detection schemes, a window of K consecutive bits obtained from the current F-bit positions aligned to by the framing circuit is examined. If x or more bits violate the F-bit pattern, the OOF condition is declared.

The Markov chain diagrams for the 3-o-o-5 and 4-o-o-7 schemes are shown in Fig. 2.6 and 2.7. Here the Markov models are used instead of the generalized state transition diagrams because the transition times of each and every transition is constant (equal to one F-bit interval). The use of Markov models enables the solving of the required values using well known matrix methods [11].

As each new bit is included (at every F-bit interval) in the K-bit examining window, there is a probability p that the new bit violates the F-bit pattern (and q = 1 - p that it does not). The transitional probabilities p and q are labelled on the branches of the Markov chain diagrams. The decimal value numbering (labelling) each state is the decimal equivalent of the binary value of the K-bit examining window (with a 1 representing an error in a bit and 0 representing no error, and the new bit is the least significant bit). Note the children states of a given state which occur somewhere else in the model are not repeated because they do not add any new information for the formation of the state transition matrix. Different states which have the same children states can be (and are) considered as identical states (e.g. states '82' and '18' in Fig. 2.7 have the same children states and therefore are identical states).

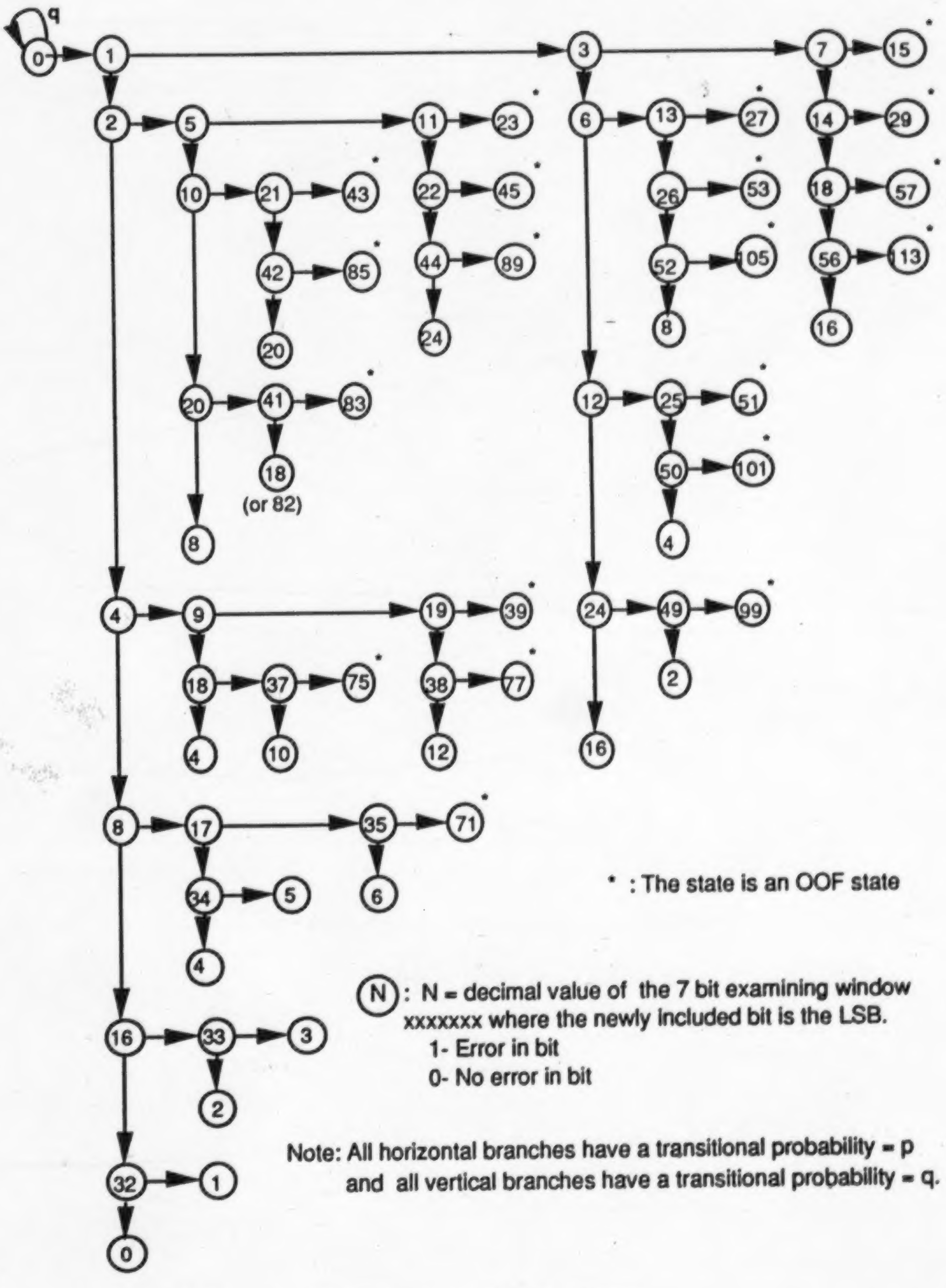
The states in Fig. 2.6 and 2.7 are renumbered into consecutive states starting from '1' and ending with a single common out-of-frame (absorbing) state. From the models with the renumbered states the state transition probability matrices are constructed and shown in Fig. 2.8. The PGF of the absorbing times between state 1 (or state 0 of Fig. 2.6 and 2.7) and the absorbing state can be derived from the state transition matrix obtained in each case. The details on how it is done are outlined in Appendix A [7].


q
P
P
P
0
1
3
7
2
5
11
10
21
20
9
8
4
9
19
18
5
4
8
17
3
2
16
1
0
6
13
12
25
24
17
16
N

* : The state is an OOF state

N = decimal value of 5 bit examining window (xxxxx) where the newly included bit is LSB
1 - error in bit
0 - no error in bit

Fig. 2.6 Markov model for the 3-o-o-5 OFD scheme.


q
0
1
3
7
15
2
5
11
23
6
13
27
14
29
10
21
43
22
45
26
53
18
57
42
85
44
89
52
105
56
113
20
24
8
16
20
41
83
12
25
51
18
(or 82)
50
101
8
4
4
9
19
39
24
49
99
18
37
75
38
77
2
4
10
12
16
8
17
35
71
34
5
6
4
16
33
3
2
32
1
0
N

* : The state is an OOF state

(N) : N = decimal value of the 7 bit examining window xxxxxxx where the newly included bit is the LSB.
1- Error in bit
0- No error in bit

Note: All horizontal branches have a transitional probability = p and all vertical branches have a transitional probability = q.

Fig. 2.7 Markov model for the 4-o-o-7 OFD scheme.

(3-o-o-5)

$$
\begin{matrix}
q & p & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & q & p & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & q & p & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & q & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & p \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & q & p & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & q & 0 & 0 & 0 & 0 & 0 & 0 & p \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & q & 0 & 0 & 0 & 0 & 0 & p \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & q & p & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & q & 0 & 0 & p \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & q & 0 & p \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & q & p \\
q & p & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & q & p & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & q & p & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & q & p & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & q & p & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0
\end{matrix}
$$

(4-o-o-7)

$$
\begin{matrix}
q & p & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & q & p & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & q & p & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & q & p & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & q & p & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & q & p & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & q & p & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & q & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & p \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & q & p & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & q & p & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & q & p & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & q & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & p \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & q & p & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & q & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & p \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & q & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & p \\
0 & p & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & q & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & q & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & p & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & q & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & p & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & q & 0 & 0 & 0 & 0 & 0 & 0 & 0 & p \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & q & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & p & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & q & 0 & 0 & 0 & 0 & 0 & p \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & q & 0 & 0 & 0 & 0 & p \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & q & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & p & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & q & 0 & 0 & p \\
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q & p & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & q & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & p \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & q & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & p \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & q & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & p \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & q & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & p \\
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0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & q & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & p \\
0 & 0 & q & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & p \\
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0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & q & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & p \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0
\end{matrix}
$$

Fig. 2.8 State transition matrices for the 3-o-o-5 and 4-o-o-7 OFD criteria.

The derived state transition probability matrices are used to analyze the OOF detection times when p and q are assigned with values of q_s and p_s respectively because an examined bit (not a F-bit during the OOF state) violates the F-bit pattern when it does not simulate this pattern (p_s is the probability of simulating an F-bit by a random bit and $q_s = 1 - p_s$ is the probability of an F-bit non-simulation).

The probability distribution of the absorbing times can be obtained by expanding the derived PGF.

The models are used to analyze the misframe times when the transition probabilities p and q are assigned with values of p_e's and q_e's respectively because an F-bit violation is actually an F-bit error during the in-frame state (where $p_e = BER_{channel}$, and $q_e = 1 - p_e$).

2.4 Statistics of the Framing Parameters

2.4.1 Steps to Obtain Statistics from a PGF

Using the PGF's ($P_X(z)$, where X is one of the timing parameters) obtained for the four framing parameters, the following operations are performed to evaluate the relevant statistical values.

i. Differentiate each $P_X(z)$ and obtain $P'_X(1)$ and $P''_X(1)$ to evaluate the mean and standard deviation of the X. See equation (2.2).

ii. Expand each $P_X(z)$ into a power series of z as shown in (2.1) and the coefficients p_0, p_1, p_2, and etc. specify the probability distribution of X. Note only the probability distributions for the MRF and OFD times can be obtained.

iii. From the probability distribution obtained in ii., useful percentile statistics (such as the 99.9 percentile value) are obtained.

2.4.2 Results

Following the steps outlined above, means and standard deviations and other percentile statistics (in the MRF and OFD cases) are obtained for the four framing parameters. The values for the MRF, FF, and OFD times (expressed in units of F-bit intervals) are shown in Table 2.1.

Table 2.1. Framing parameters for conventional DS3 framing.

	Mean	Standard Deviation	99.5 percentile	99.8 percentile	99.9 percentile
MRF[1]	359	18.4	409	416	420
FF[2]	$2.1 * 10^6$	$2.1 * 10^6$	N/A	N/A	N/A
OFD (3-o-o-5)	7.27	4.66	28	32	35
OFD (4-o-o-7)	9.85	6.06	37	42	46

P_F (c=20, BER = 10^{-6}) = 0.00016115.

The values of T_{MF}[3] (or their logarithms), in units of F-bit intervals and in actual time for BER ranging from 10^{-4} to 10^{-10} are as follows:

Table 2.2 Misframe times of conventional DS3 framing.

Log(BER)	-4	-5	-6	-7	-8	-9	-10
Log(T_{MF}) (3-o-o-5)	11.2 (7 days)	14.2 (19.4 yrs)	17.2 ($1.9\ 10^4$ yrs)	20.2 ($1.9\ 10^7$ yrs)	23.2 ($1.9\ 10^{10}$ yrs)	26.2 ($1.9\ 10^{13}$ yrs)	29.2 ($1.9\ 10^{17}$ yrs)
Log(T_{MF}) (4-o-o-7)	14.7 (61.2 yrs)	18.7 ($6.1\ 10^5$ yrs)	22.7 ($6.1\ 10^9$ yrs)	26.7 ($6.1\ 10^{14}$ yrs)	30.7 ($6.1\ 10^{18}$ yrs)	34.7 ($6.1\ 10^{22}$ yrs)	38.7 ($6.1\ 10^{26}$ yrs)

The probability distributions for the MRF and OFD times are obtained by expanding their respective PGF's and are plotted in Fig 2.9 and 2.10.

The framing parameter values tabulated in Table 2.1 and Table 2.2 serve as a bench mark against which those of the FEC framing are compared.

---

[1] The statistics of the MRF time vary insignificantly as BER ranges from 10^{-6} to 10^{-11}.

[2] The standard deviation of the FF time is identical to that of its mean value.

[3] The standard deviation of the MF times are identical to those of their mean value.

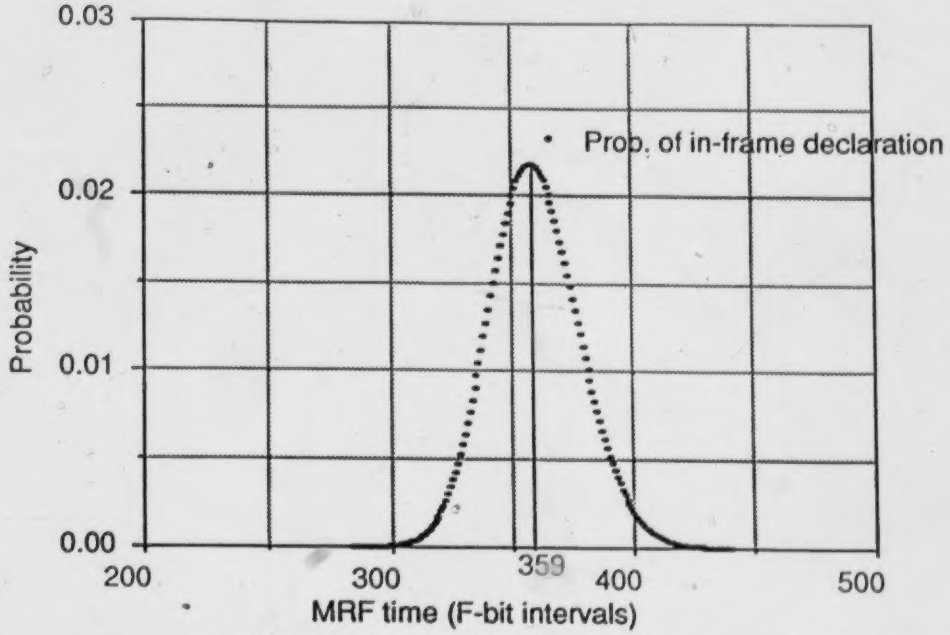

Fig. 2.9 Probability distribution of MRF times for F-bit framing (c=20).

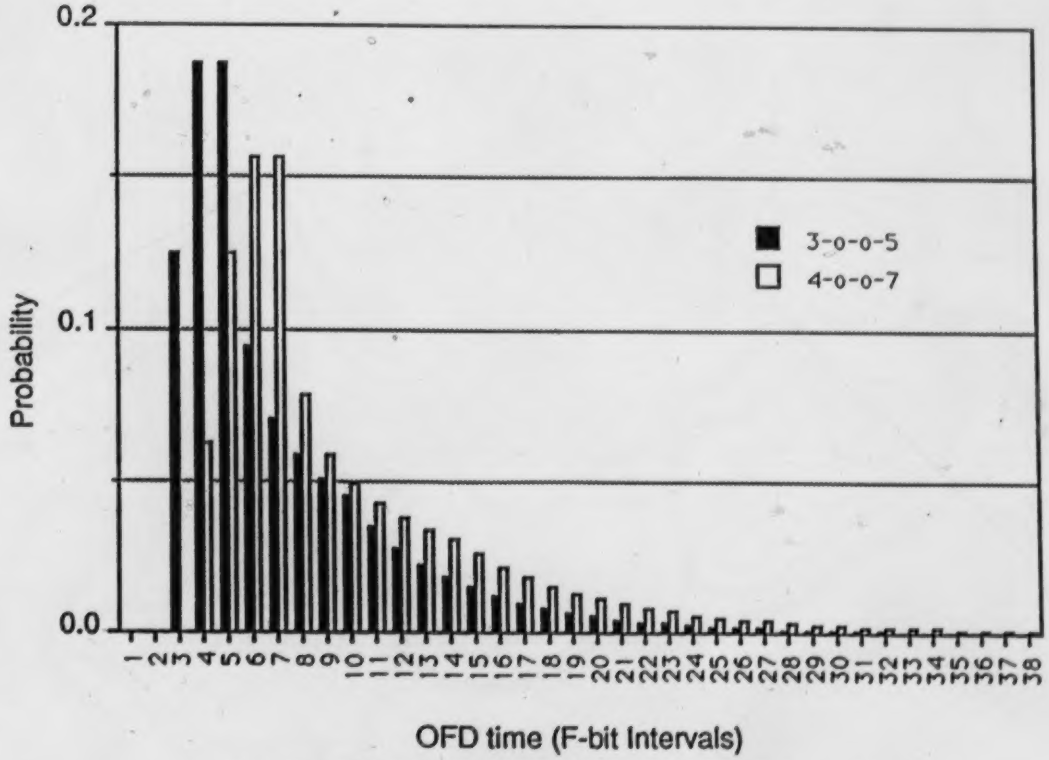

Fig. 2.10 Probability distributions of the OFD times for the
3-o-o-5 & 4-o-o-7 OFD schemes.

3. COMBINED FRAMING AND FEC CODING

3.1 Selection of the FEC Code

As outlined in the introduction, the combined framing and FEC scheme can be achieved by first coding each (appropriately sized) block of DS3 data (without the F-bits) into FEC data bits and replacing the F-bits with FEC check bits. The design of the FEC code requires the selection of:

i. The type of code to be used.

ii. The number of bits in each frame that can be freed up and reused as parity check bits.

iii. The block size of the FEC code.

The basic structure of the DS3 frame is as follows:

$$V\ [84]\ F_1\ [84]\ C_{i1}\ [84]\ F_0\ [84]\ C_{i2}\ [84]\ F_0\ [84]\ C_{i3}\ [84]\ F_1\ [84]$$

where V = X, P or M bit; C_{i1}, C_{i2}, C_{i3} are the C_i bits (triplicated stuffing control bits for the i-th tributary); F_1, F_0 are the F-bits (the primary framing bits); and [84] denotes the payload bits.

The C bits are triplicated to provide a single error correction capability. If the FEC code is implemented, each coded frame will also have this capability. Hence, the C bit triplication is unnecessary. The normally redundant C_{i2} and C_{i3} bits can then be reused as parity check bits of the FEC code.

As a result , the total number of freed F and C bit slots for each frame (of 680 bits) becomes six. This implies a code rate of 98.82% is required. A rate higher than 98%, together with implementation simplicity consideration, suggest the use of a Hamming code. Further discussion of the type of codes for the intended applications is found in [3].

3.1.1 Hamming Codes

Hamming codes are linear cyclic codes which have the attractive property that their encoding and decoding operations can be easily implemented using shift registers with feedback connections [12].

An (n,k) Hamming code satisfies the relation:

$$(n,k) = (2^m - 1, 2^m - m - 1) \tag{3.1}$$

where n is the length of code words including data and check bits (it is also called the block size) and k is the length of message block in bits. n-k = m is the number of check bits. The check bits polynomial p(x) is defined as:

$$p(x) = [x^{n-k} m(x)] \bmod g(x) \tag{3.2}$$

where m(x) is the message polynomial and g(x) is the irreducible generator polynomial. Each code word c(x) in systematic form is formed by concatenating p(x) to the end of the message:

$$c(x) = x^{n-k} m(x) + p(x) \tag{3.3}$$

All Hamming codes have single error correcting (SEC) capability. In addition, one extra overall parity check bit can be added to the basic Hamming code word, changing the structure to:

$$(n,k) = (2^m, 2^{m-1} - m - 1) \tag{3.4}$$

This is called the extended Hamming code, which in addition to the SEC capability, also has double error detection (DED) capability.

In system design, if a code of suitable natural length cannot be found, it may be desirable to shorten a code to meet the requirements. The shortening of an (n,k) code is done by setting the *l* leading information digits to zero, or in practice the *l* leading bits are not transmitted at all because they contain no information. The shortened code then becomes (n-*l*, k-*l*). The encoding and decoding process for a shortened code can be accomplished by the same circuits as those employed by the original code. This is because the deleted *l* leading-zero information digits do not affect the parity-check and syndrome computations.

3.1.2 The FEC Code for the DS3 Signal (DS3-FEC Code)

Applying the Hamming code structure rule described above, it was found that every two consecutive frames can be combined into a (1360, 1348) extended code word (shortened from the parent extended Hamming code (2048, 2036)). This is the same type of code proposed for SONET, using unallocated existing overheads, in [2]. This code has single error correction (SEC) and double error detection (DED) capabilities. The resulting FEC code word structure is as follows:

V [84] r_1 [84] C_i [84] r_2 [84] r_3 [84] r_4 [84] r_5 [84] r_6 [84]

V [84] r_7 [84] C_j [84] r_8 [84] r_9 [84] r_{10} [84] r_{11} [84] p [84]

where V = X, P or M bit; C_i, C_j are the first C bits of the ith and jth frame respectively; r_1 (the highest order check bit), r_2, ... , r11 are the parity check bits of the original Hamming code; p is the even parity bit of the extended code; and [84] denotes the payload bits.

The following irreducible (and primitive) polynomial was selected as the generator polynomial for the code [13]:

$$g(x) = x^{11} + x^2 + 1 \qquad (3.5)$$

3.2 The Encoder for the DS3-FEC Code

The schematic diagram for the encoder of the FEC code is shown in Fig. 3.1.

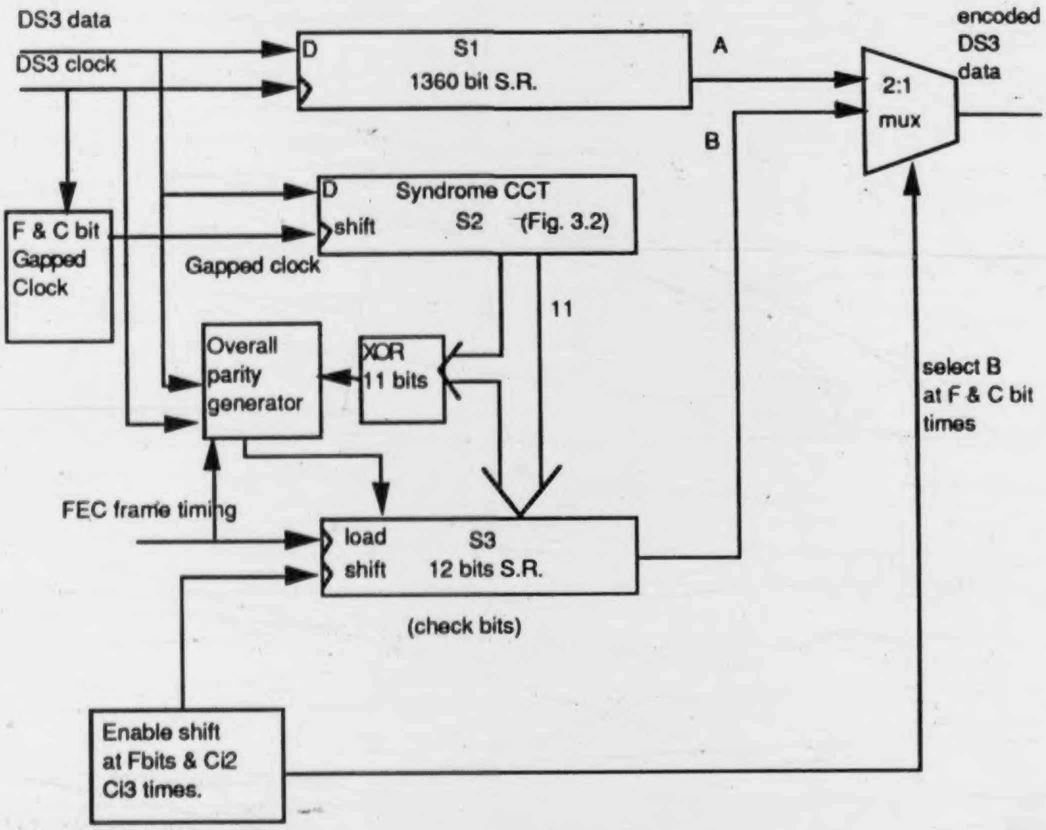
DS3 data
DS3 clock
D
S1
1360 bit S.R.
A
B
encoded
DS3
data
2:1
mux
D
Syndrome CCT
shift
S2
(Fig. 3.2)
F & C bit
Gapped
Clock
Gapped clock
11
Overall
parity
generator
XOR
11 bits
select B
at F & C bit
times
FEC frame timing
load
shift
S3
12 bits S.R.
(check bits)
Enable shift
at Fbits & Ci2
Ci3 times.

Fig. 3.1 Encoder for the DS3-FEC code.

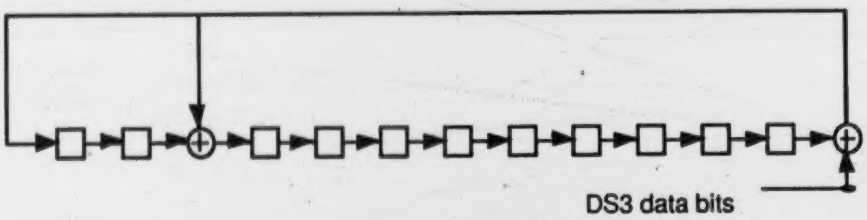
DS3 data bits

Fig. 3.2 Parity check bits generator circuit for the DS3-FEC code.

The encoding of the DS3-FEC code involves two steps. First, all the data bits (except the F, Ci2, and Ci3 bits) are shifted through the syndrome circuit S2 (Fig. 3.2). This is controlled by the "Gapped Clk" unit which disables the shifting of the F, Ci2, and Ci3 bits through the syndrome circuit S2. The two DS3 frames of data are stored in the delay buffer S1 until the check bits and the overall parity bit for them are generated and transfered in parallel to register S3. The bits in S1 are sequentially shifted out (for transmission). The bits in the F, Ci2, and Ci3 bit slots are not transmitted; instead at those times the parity check bits $r_1, .., r_{11}, p,$ stored in S3 are transmitted. The timing and control of this process is driven by the "Enable Shift" unit which generates enable signals at the appropriate F, Ci2, and Ci3 bit timings to enable the transmission of the check bits.

The encoding delay incurred by the FEC encoding process is:

$$(1360/44.736 \text{ Mbs}) = 30.4\ \mu\text{sec} \tag{3.6}$$

which is negligible for most applications.

3.3 Decoding the DS3-FEC Code.

3.3.1 Error-pattern Detection for Shortened Codes

Before performing error location and correction on the received word R(x) at the receiver, the syndrome S(x) is obtained by dividing R(x) by g(x).

$$S(x) = R(x) \bmod g(x).$$

When a full length (n,k) code is used, the computed syndrome S(x) is used to detect whether an error has occurred in the leading (most significant) bit (MSB). This is done by having an error-pattern detection circuit which decodes for a syndrome pattern equivalent to $x^{n-1} \bmod g(x)$. However, in shortened codes the leading l information bits are deleted. In order to detect an error in the leading bit of a shortened code, the error-pattern detection circuit must be modified to decode for a pattern equivalent to x^{n-l-1} mod $g(x)$ [12]. For the shortened DS3 code, the pattern to be decoded is:

$$Se(x) = x^{1358} \bmod (x^{11} + x^2 + 1) = x^{10} + x^9 + x^2 \text{ (or } = 604_H) \tag{3.7}$$

We have just described the mechanism for detecting whether an error has occurred in the leading bit. The following section will describe the mechanism for the decoding operation of all the bits in the code word. It is based on the Meggitt decoder [12] with minor modifications for the shortened and distributed DS3 code.

3.3.2 The Decoder

The decoder for the DS3 code is shown in Fig. 3.3. The received data of a frame (code word) is stored in a delay buffer while the syndrome for the received frame is computed by the syndrome circuit S1 (the syndrome circuit for the distributed DS3 code will be described in detail in Sec. 3.5). At the end of the frame (period) the syndrome for the frame is generated. If the generated syndrome is non-zero and the overall check-sum is odd, the error correction unit (ECU) is activated to locate and correct a single error in the frame.

To perform the error location and correction, the syndrome computed in S1 is loaded in parallel onto the syndrome circuit S2 (which is a normal syndrome circuit, depicted in Fig. 3.4, with a preset load mechanism) in the ECU, and its pattern is checked by an error-pattern detection circuit to determine whether the most significant bit (MSB) is in error. If it is, an error correction signal is generated to correct the MSB to be read out.

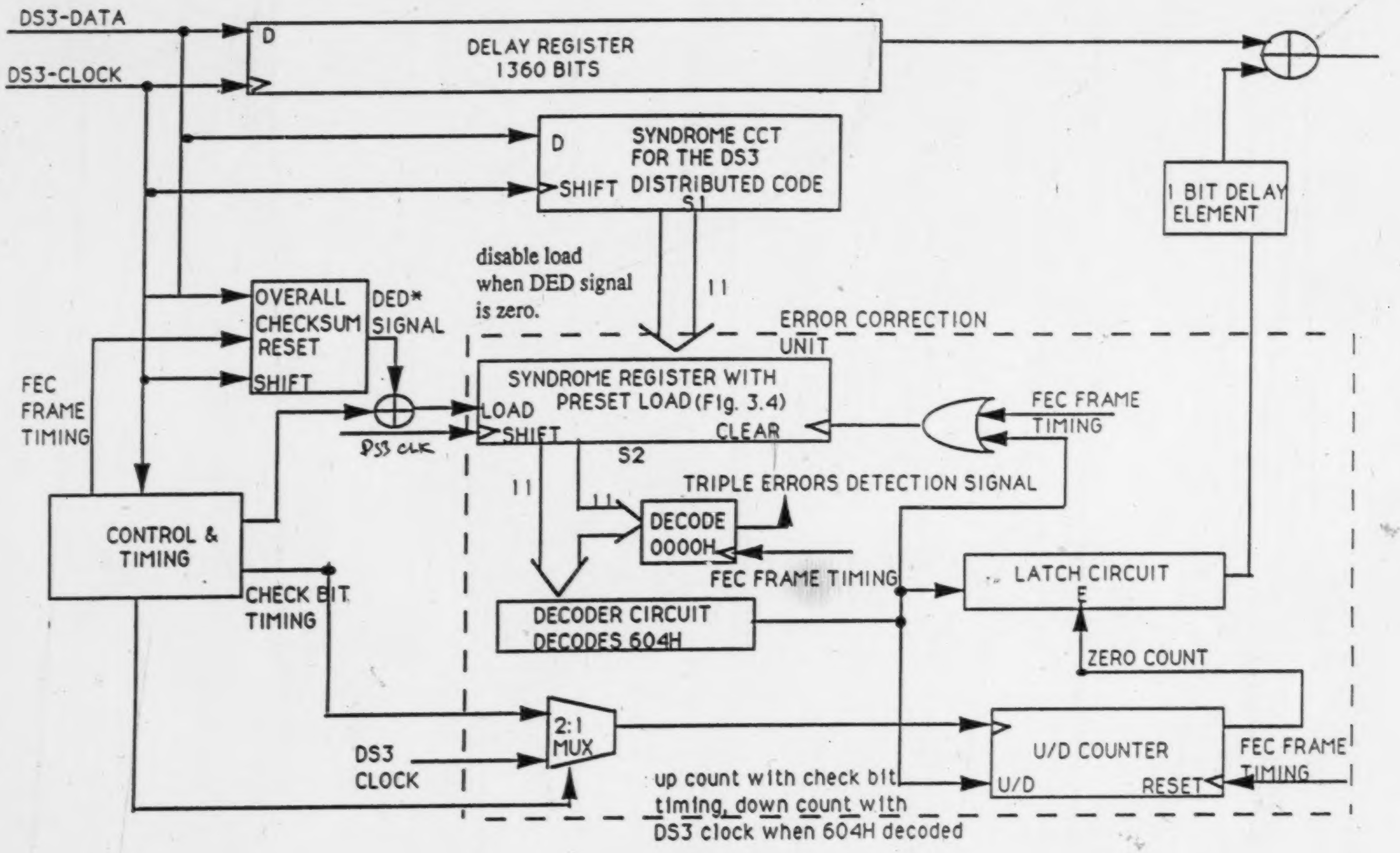
DS3-DATA
DS3-CLOCK
D
DELAY REGISTER
1360 BITS
D
SYNDROME CCT
FOR THE DS3
SHIFT
DISTRIBUTED CODE
S1
1 BIT DELAY
ELEMENT
disable load
when DED signal
is zero.
11
OVERALL
CHECKSUM
RESET
SHIFT
DED*
SIGNAL
ERROR CORRECTION
UNIT
FEC
FRAME
TIMING
SYNDROME REGISTER WITH
PRESET LOAD (Fig. 3.4)
LOAD
SHIFT
CLEAR
DS3 CLK
FEC FRAME
TIMING
S2
11
11
TRIPLE ERRORS DETECTION SIGNAL
DECODE
0000H
CONTROL &
TIMING
FEC FRAME TIMING
LATCH CIRCUIT
E
CHECK BIT
TIMING
DECODER CIRCUIT
DECODES 604H
ZERO COUNT
2:1
MUX
U/D COUNTER
U/D
RESET
FEC FRAME
TIMING
DS3
CLOCK
up count with check bit
timing, down count with
DS3 clock when 604H decoded

Fig. 3.3 Decoder circuit for the DS3-FEC code.

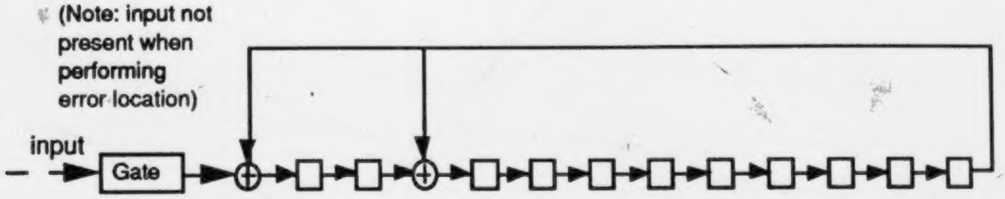

Fig. 3.4 Syndrome circuit for the DS3-FEC code.

Before each subsequent bit in the delay buffer is read out (into the demultiplexer), the syndrome circuit S2 evaluates a new syndrome by dividing the syndrome obtained in the previous bit time and its error-pattern detection circuit checks whether the new syndrome is the one that corresponds to an error in the current right most bit of the received buffer. As before if it is in error an error correcting signal is generated to correct the erroneous bit being read out. The same signal also resets the content of S2 to zero to prevent any further error correction.

The error correction method described above can only correct a single error that has occurred in a frame. For frames with double errors, the overall check-sum of the frame becomes even, hence no error correction is attempted (i.e. the ECU is not loaded with the FEC syndrome). For frames with multiple odd errors (a non-zero syndrome and an odd check-sum), the decoder will assume a single error has occurred and will perform a (generally) wrong error correction attempt at the location specified by the syndrome. (This causes error multiplication.) For the full length (parent) code a correction location is always located using the non-zero syndrome (obtained from multiple odd errors); this is because every non-zero syndrome is associated with an erroneous position in the word. However, for shortened codes, a correction location is not always located using the syndrome computed for frames with multiple odd errors. This is because some of the computed non-zero syndromes are actually associated with an erroneous position outside the shortened word. In these cases the ECU will fail to locate an erroneous position in the frame, and the syndrome of the ECU will remain non-zero at the end of the frame period (when the last digit of the frame in the delay buffer has been read out). When this happens, the ECU can interpret that at least 3 errors must have occurred in the previous frame period. Therefore, the detection of some frames with triple errors for shortened codes is possible by checking for a non-zero content in the syndrome of the ECU at the end of each frame period. This is implemented by using a detection circuit which decodes for a non-zero syndrome (in S2) every frame period and sets the triple error detection signal when the syndrome in S2 is non-zero (see Fig. 3.3).

The single, double and sometimes triple error detecting capabilities characteristic of the decoding of shortened codes can be used by the OOF detection circuit to speed up the OOF detection process. This will be discussed in Chapter 5.

The decoder just described assumes that all the data bits are contiguous and the error correction signal generated at each shift corresponds to the bit being read out. However, for the distributed codes the data bits are separated (gapped) by distributed parity check bits at 12 different positions. The continuous generation of error correction signals by shifting S2 continuously would create differences between the timing of the generated error correction signal and the timing of the bit being read out of the received buffer. One way of compensating for these timing differences is by disabling the shifts of S2 at each parity check bit time. (That is clocking S2 with a gapped DS3 clock). However, this method has the disadvantage that the error location and correction process can only be completed in 1360+12 bit times and triple error detections are not available at the end of a frame period. This implies two staggered syndrome circuits are needed (with each one decoding alternate FEC frames). A more efficient way of decoding the distributed code is by shifting S2 continuously as if the data bits were contiguous. This means the required gaps in the shifting at the parity check bit times are eliminated. Using this method, the timing of the error correction signal generated at each shift for the first 85 bits (before the first check bit time) of the frame correctly corresponds to the timing of the bit being read out. But at the 86th shift (i.e. the first check bit time), the error correction signal generated should actually be used for the (possible) error correction of the 87th output bit (which is the 86th data bit) of the buffer. This one bit time difference between the timing of the error correction signal and the output bit of the received buffer (word) persists until the 256th shift (i.e. the second parity check bit time). The error correction signal generated at the 256th shift should actually be used to locate any error at the 258th output bit of the buffer. Therefore, after the 256th shift, a two bit time difference exists between the timing of the error correction signal and the output bit of the buffer. Similarly, each time the clock cycle shifts pass a check bit time this time difference is increased by an additional bit time. When no error is located, (i.e. the error correction signal is zero) the time difference can be maintained by an up/down (u/d) counter which increments its count at each check bit time. When an error is located, and if the u/d counter has a non-zero value, the error correction signal cannot be used immediately to correct the current output bit, instead a number of bits specified by the counter has to elapse before the error correction signal is used. This can be implemented by feeding the error correction signal through a latch circuit with its latching action triggered by the zero-count output of an u/d counter. The counter should start down counting, according to the DS3 clock timing, as soon as the error correction signal has a high logic state and down count to zero to effect the latching action.

3.4. FEC Framing

As described in the introduction, the FEC framing scheme uses the information of syndromes produced by the FEC decoder to perform the function of framing (reframing and OOF detection). Firstly, for out-of-frame detection, the decoder examines a frame of n newly received bits, as if it had a receiving window n bit wide, and produces a syndrome for the frame. A syndrome is produced for each newly received frame every n-bit time. The framing circuit examines the computed syndrome to see if it contains only zero bits (a zero syndrome). If the syndrome contains some non-zero bits (a non-zero syndrome), then the OOF detection count is incremented. If a predetermined number, c, of consecutive non zero syndromes is reached the framing circuit declares the OOF condition.

Once out-of-frame, the framing circuit signals a modified decoder to initiate the search process and scan for the frame alignment boundaries. The modified decoder then slides its n-bit wide window along, one bit at a time, by including the newly received bit and discarding the oldest bit of the window. A syndrome is generated for the current bits in the window every bit time (i.e. as each new bit arrives) and examined by the framing circuit. This bit-time sliding and computation of syndromes continues until a zero syndrome has been computed. When this happens, the framing circuit temporarily accepts the current boundaries of the received window as the frame boundaries and calls in the confirmation process. The framing circuit then checks if zero syndromes are produced for subsequent frames. (Again a confirmation test is needed, because at times the block of bits obtained from a non-aligned frame can mimic a valid FEC code word and yield a zero syndrome. During the confirmation phase, the framing circuit only checks the syndromes produced at n bit or frame intervals.) If this is not the case, the modified decoder continues the bit-by-bit syndrome computation and checking process. When a predetermined number, c, of consecutive zero syndromes are decoded for the last c received frames, the framing circuit declares itself frame aligned.

A modified decoder is required which computes an updated syndrome every bit time to determine whether a bit position is the frame boundary, because a conventional decoder only computes a syndrome every n bit times (n is the number of bits in the FEC frame).

Specifically, the maximum length search for the in-frame position using a normal decoder will take approximately (n-1)*n bit times because an entire group of bits equal to the code block size must be evaluated for each candidate bit position. To complete the same search using a modified decoder will only take approximately n bit times. The modified decoder will significantly reduce the search time, roughly by a factor of n (= 1360 for our code). That is, the search time is reduced from 4.1msec to around 3 μsec.

3.5 Fast Framing by Continuously Compensated Syndrome Computation (CCSC)

The modified decoders for the various code word formats of interest (with different parity check bit placements, and also the shortened and extended code formats) are presented in this section. The probability of mimic for each format considered is also analyzed to facilitate the analysis of framing parameters in Section 3.8.

3.5.1 Systematic (n,k) Code

To compute a syndrome for the word in an n-bit sliding window every bit time, modifications to the syndrome computation circuit normally used in a conventional decoder are required. The continuously compensated syndrome computation (CCSC) can be implemented because of the cyclic nature of Hamming codes, and its explanation is given below.

Let $R_i(x)$ be the polynomial corresponding to some n consecutive bits, and $R_{i+1}(x)$ be the polynomial corresponding to the n consecutive bits obtained from $R_i(x)$ by including the next (newly received) bit and discarding the oldest bit of $R_i(x)$. $R_{i+1}(x)$ can be considered as the adjacent word of $R_i(x)$. Let $R_i(x)$ and $R_{i+1}(x)$ be:

$$R_i(x) = a_n x^{n-1} + a_{n-1} x^{n-2} + \dots + a_2 x + a_1 \qquad (3.8)$$

and

$$R_{i+1}(x) = a_{n-1}\, x^{n-1} + a_{n-2}\, x^{n-2} + \ldots + a_1\, x + a_0 \tag{3.9}$$

where a_0 is the newly received bit. Combining (3.8) and (3.9) we have,

$$R_{i+1}(x) = x\, R_i(x) + a_n\, x^n + a_0 \tag{3.10}$$

Let the syndrome of $R_i(x)$ be:

$$S_i(x) = R_i(x) \bmod g(x) \tag{3.11}$$

where $g(x)$ is the generator polynomial. Then the syndrome $S_{i+1}(x)$ of $R_{i+1}(x)$ can be obtained by dividing both sides of equation (3.10) by $g(x)$:

$$S_{i+1}(x) = x\, R_i(x) \bmod g(x) + a_n\, x^n \bmod g(x) + a_0 \tag{3.12}$$

Note that $a_n\, x^n \bmod g(x) = a_n$. It is also known [12] that

$$x\, R_i(x) \bmod g(x) = x\, S_i(x) \bmod g(x) \tag{3.13}$$

Hence, the syndrome of $xR_i(x)$, (or $xS_i(x)$) can be computed in a normal syndrome circuit by shifting its initial content $S_i(x)$ once, while disabling (isolating) the input gate. Equation (3.12) can then be rewritten as:

$$S_{i+1}(x) = x\, S_i(x) \bmod g(x) + a_n + a_0 \tag{3.14}$$

Equation (3.14) demonstrates that the evaluation of a syndrome for a given bit time can be obtained by shifting that obtained at the previous bit time through the syndrome circuit and adding (modulo-2) a_n and a_0. Fig. 3.5 shows an implementation of (3.14) for a (15,11) code (with $g(x) = x^4 + x + 1$).

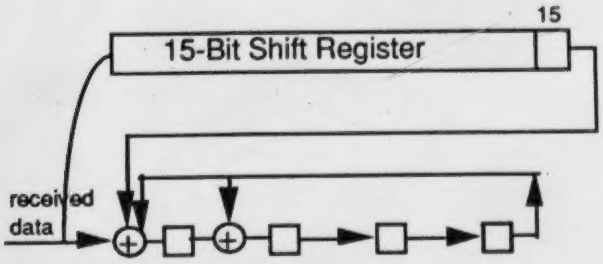

Fig. 3.5 CCSC scheme for a systematic (15,11) code.

As described earlier the framing circuit is looking for zero syndromes when scanning for the frame alignment position. However, occasionally zero syndromes might be obtained for misaligned positions. This is because random data in misaligned words occasionally mimics valid code words. The probability of such mimic is denoted as p_m. In fact in systematic codes p_m ranges from 1/2 to 2^{k-n} and its value decreases exponentially with the magnitude of shift of the misaligned word from the aligned position. To demonstrate this, let $S_i(x)$ be the zero syndrome of an aligned word $R_i(x)$, and $S_{i+1}(x)$ be the syndrome of a misaligned word $R_{i+1}(x)$ formed as a result of a one-bit shift. From (3.14) $S_{i+1}(x)$ will also be equal to zero if $a_n = a_0$. The probability of $a_n = a_0$ is 1/2 for random data. Therefore, $p_m = 1/2$ for a shift of one bit and the value of p_m is reduced by a factor of 2 with each additional shift. Therefore, p_m can be expressed as a function of the magnitude of the shift, d, as follows:

$$p_m(d) = \begin{cases} \left(\frac{1}{2}\right)^{|d|} & ; |d| \le (n - k). \\ \left(\frac{1}{2}\right)^{n - k} & ; |d| \ge (n - k). \end{cases} \tag{3.15}$$

Note that the lowest value of p_m is $(1/2)^{n-k}$, which is the probability of a block of random bits of length n mimicking a valid code word. p_m as high as 1/2 is undesirable for the reframe and out-of-frame processes, because it causes excessive mimics at misaligned positions which increase the probability of false declaration of the in-frame state, and increases the reframe and out-of-frame detection times. The values of p_m for a (31,26) systematic code obtained experimentally using computer simulations are plotted in Fig.3.6.

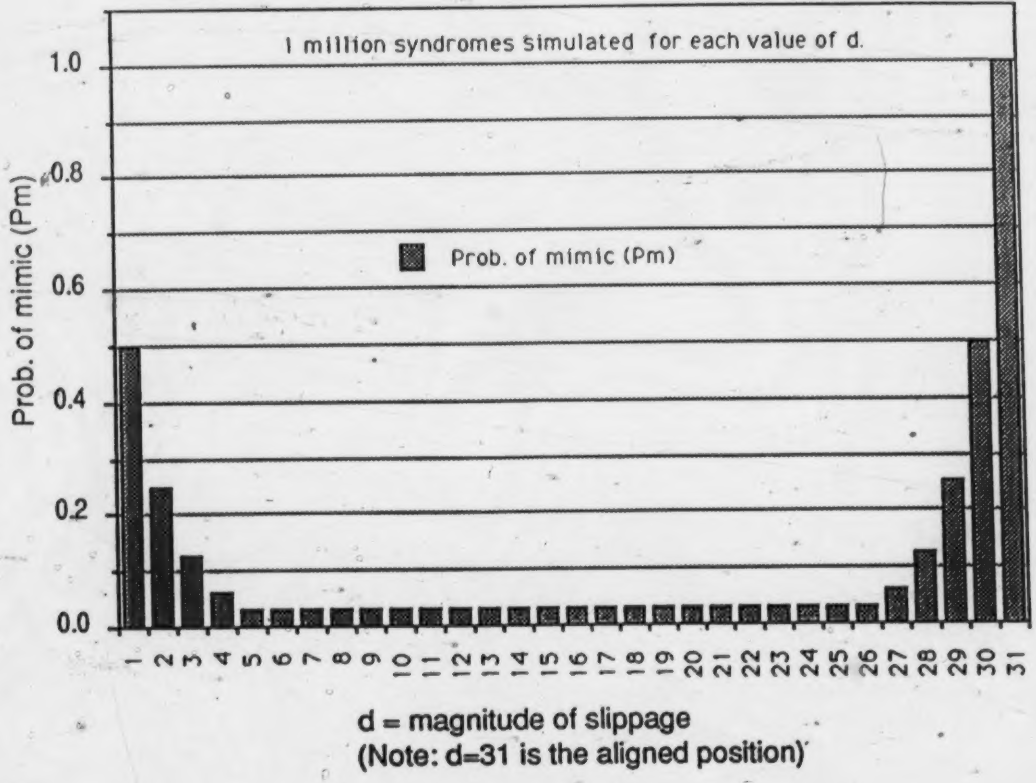

Fig. 3.6 Prob. of mimic vs d (magnitude of slippage) for the (31,26) Hamming code.

3.5.2 Shortened and Extended Systematic Code

Consider an (m+1, k-l+1) extended shortened code, where m = n - l. Let R_i = (a_{m+1}, a_m, . . . , a_2, a_1) be a vector representing the block of bits in a (m+1) bit receiver buffer at an arbitrary time i. Let $R_i(x)$ be the polynomial formed from R_i in the following way:

$$R_i(x) = a_{m+1}\, x^{m-1} + a_m\, x^{m-2} + \ldots + a_3\, x + a_2 \qquad (3.16)$$

At time i+1, the buffer contains R_{i+1} = (a_m, a_{m-1}, . . ., a_2, a_1, a_0) with a_0 being the newly received bit.

Similarly,

$$R_{i+1}(x) = a_m\, x^{m-1} + a_{m-1}\, x^{m-2} + \ldots + a_2\, x + a_1 \qquad (3.17)$$

Note that a_1 and a_0 are the overall parity bits at time i and i+1, and they are not included in equations (3.16) and (3.17).

Combining (3.16) and (3.17), we get

$$R_{i+1}(x) = x\, R_i(x) + a_{m+1}\, x^m + a_1 \qquad (3.18)$$

Dividing both sides of (3.18) by g(x) and equating the remainders we obtain,

$$S_{i+1}(x) = x\, S_i(x) \bmod g(x) + a_{m+1}\, x^m \bmod g(x) + a_1 \qquad (3.19)$$

Now x^m mod g(x) is a fixed polynomial of degree less than n-k and it can be precomputed (prewiring the non-zero bits), multiplied by a_{m+1} and added to $xS_i(x)$ mod g(x) and a_1 to produce $S_{i+1}(x)$. Similarly, to have a mimic (zero syndrome) for a shift of 1 bit requires zero values for both a_{m+1} and a_1. The probability of having such an occurrence for random data is 1/4. Again p_m is reduced by a factor of 1/4 with each additional shift. Therefore, p_m for this case expressed as a function of d is given by:

$$P_m(d) = \begin{cases} \left(\frac{1}{2}\right)^{2|d|} & ; |d| \le \frac{(n-k)}{2}. \\ \left(\frac{1}{2}\right)^{n-k} & ; |d| \ge \frac{(n-k)}{2}. \end{cases} \tag{3.20}$$

where d is the magnitude of the shift from the true aligned position. The values of p_m for a (30,24) shortened and extended code obtained using computer simulations are plotted in Fig. 3.7. The simulated results are consistent with theoretical values of (3.20).

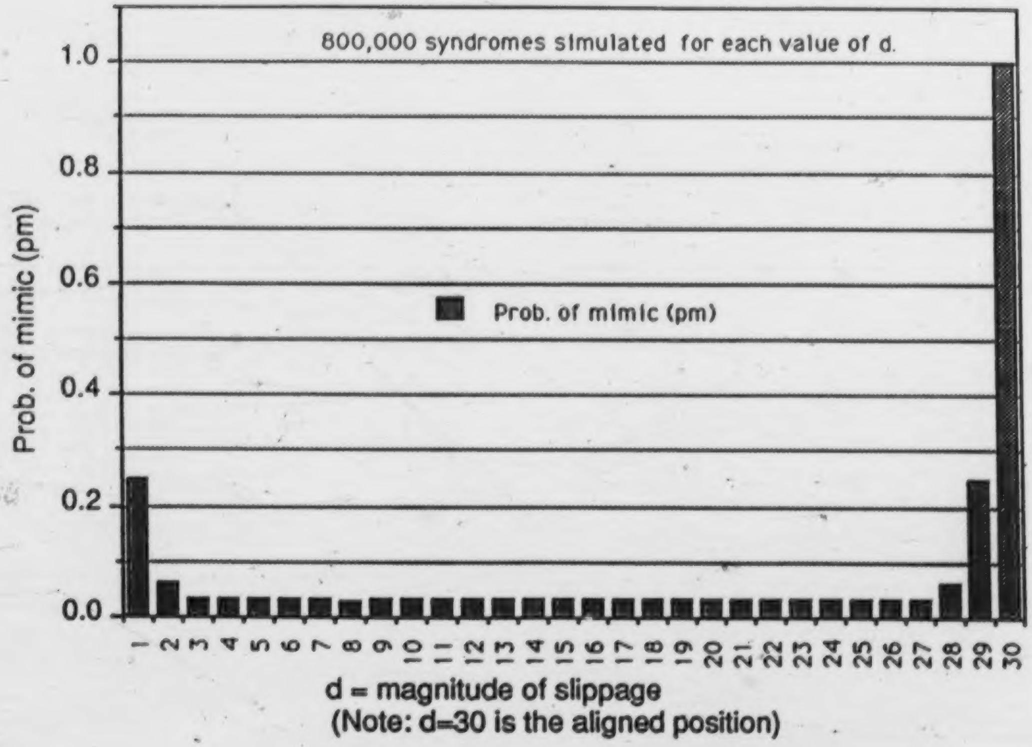

Fig. 3.7 Prob. of mimic vs d (magnitude of slippage) for the (30,24) shortened & extended Hamming code.

3.5.3 Shortened and Extended Systematic Reversed Code (with Parity Check Bits in Reversed Order)

Values of Pm higher than the minimum can be eliminated if more differing positions between the left shift of block R_i and R_{i+1} are created. This can be done by arranging and transmitting the check bits of each code word in a reversed order. We shall call this type of code the systematic reversed code (i.e. the code is still a systematic one except its parity check bits are arranged in a reversed order). At the receiver the bits at the check bit positions of the buffer are used in a reversed order so as to reconstruct the systematic form of the receiver word. For an (m+1, k-l+1) code, let $Rrev_i = (a_{m+1}, a_m, \dots a_2, a_1)$ be the bits in the receiver buffer at an arbitrary time i. The systematic form of $Rrev_i$ is $R_i = (a_{m+1}, a_m, \dots, a_{n-k+2}, a_2, a_3, a_4, \dots, a_{n-k}, a_{n-k+1}, a_1)$. Correspondingly,

$$R_i(x) = a_{m+1}\, x^{m-1} + a_m\, x^{m-2} + \dots + a_{n-k+2}\, x^{n-k} +$$

$$a_2\, x^{n-k-1} + a_3\, x^{n-k-2} + \dots + a_{n-k}\, x + a_{n-k+1} \qquad (3.21)$$

Similarly, at time i+1, $R_{i+1} = (a_m, a_{m-1}, \dots, a_{n-k+1}, a_1, a_2, \dots, a_{n-k}, a_0)$ and

$$R_{i+1}(x) = a_m\, x^{m-1} + a_{m-1}\, x^{m-2} + \dots + a_{n-k+2}\, x^{n-k+1}$$

$$+ a_{n-k+1}\, x^{n-k} + a_1\, x^{n-k-1} + a_2\, x^{n-k-2} + \dots +$$

$$a_{n-k-1}\, x + a_{n-k} \qquad (3.22)$$

Note that a_1 and a_0 are the overall parity bits at time i and i+1, they are not part of the syndrome computation process and are therefore not included in equations (3.21) and (3.22).

Combining (3.21) and (3.22) we have,

$$R_{i+1}(x) = x\, R_i(x) + D(x) \qquad (3.23)$$

where

$$D(x) = a_{m+1} x^{m} + (a_2 + a_{n-k+1}) x^{n-k} + (a_3 + a_1) x^{n-k-1} +$$

$$(a_4 + a_2) x^{n-k-2} + \ldots + (a_{n-k+1} + a_{n-k-1}) x + a_{n-k} \quad (3.24)$$

From (3.23),

$$S_{i+1}(x) = x\, S_i(x) \bmod g(x) + D(x) \bmod g(x) \quad (3.25)$$

Now $x^m \bmod g(x)$ and $x^{n-k} \bmod g(x)$ are some fixed polynomials of degree less than n-k and can be precomputed (prewiring the non-zero bits), multiplied respectively by a_{m+1} and $(a_2 + a_{n-k+1})$, and added to $x\, S_i(x) \bmod g(x)$. The other coefficients of D(x) are obtained as the sum the appropriate pairs of bits in the receiver buffer, and then they are also added to $xS_i(x) \bmod g(x)$ to produce the final value of $S_{i+1}(x)$.

To deduce p_m for the misaligned word resulting from a one-bit shift, let $S_i(x)$ be the zero syndrome of a valid code word $R_i(x)$. Then the syndrome $S_{i+1}(x)$ of the word $R_{i+1}(x)$ obtained as a result one shift (d=1) is also equal to zero if D(x) mod g(x) is zero (from (3.25)). The polynomial D(x) has n-k+2 terms, the coefficient of each term is determined by the random values of the appropriate (pair of) bits (a_{m+1}, a_{n-k+1}, a_{n-k-1},..., and etc). Since there are more than n-k random terms in D(x), the probability that it forms a valid code word is equal to 2^{k-n} (this value is dictated by the inherent redundancy of the FEC code, which is the same as the probability of a block of random bits mimicking a valid code word. Therefore, $p_m = (2)^{k-n}$ at d = 1. Similarly, it can be shown that value of p_m for all magnitudes of shift is also equal to $(1/2)^{n-k}$. The values of p_m (as a function of d) for a shortened and extended (1360,1348) systematic reversed code obtained using computer simulations are plotted in Fig. 3.8. Once again the simulated results are consistent with the theoretical ones.

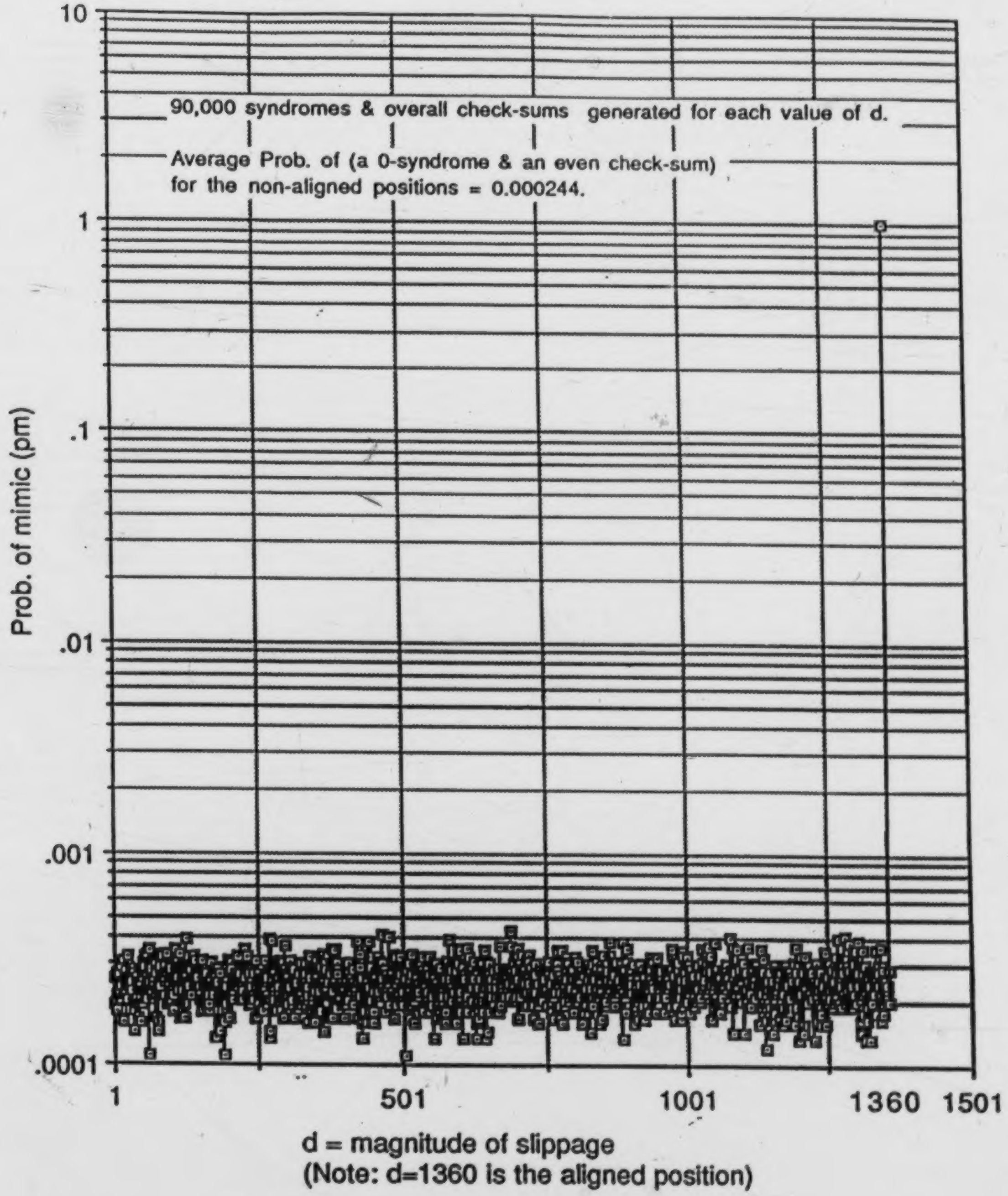

Fig. 3.8 Prob. of mimic vs d (magnitude of slippage) for the (1360,1348) systematic reversed code.

A possible implementation of (3.25), for a (12,7) code using $g(x) = x^4 + x + 1$ (as an example), is shown in Fig. 3.9.

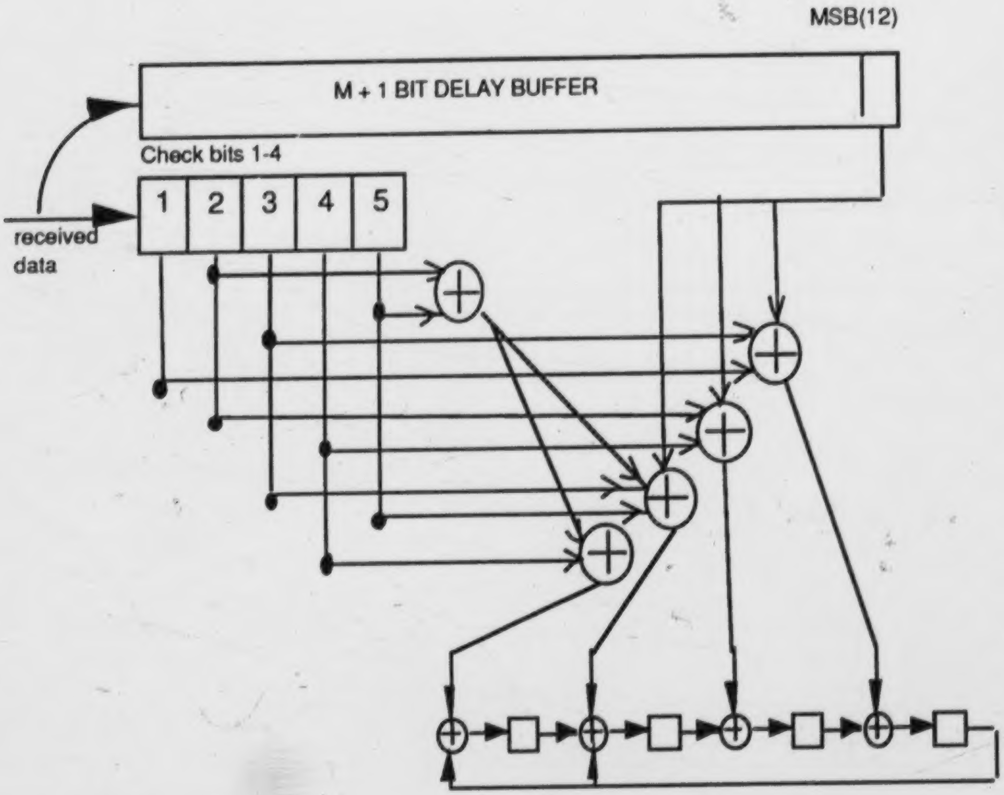
MSB(12)
M + 1 BIT DELAY BUFFER
Check bits 1-4
1
2
3
4
5
received data

Fig. 3.9 CCSC circuit a systematic reversed (12,7) code.

In general, the relationship between $S_{i+1}(x)$ and $S_i(x)$ can be devised, for whatever method of placement of parity check bits. That relationship can be obtained by deriving the expression for the polynomial $D(x)$ which is the difference between $R_{i+1}(x)$ and $xR_i(x)$ The equivalent difference vector D can be obtained from the vectors R_{i+1} and the left shift of R_i.

3.5.4 The DS3-FEC code (with Distributed Placement of Check Bits)

The general equation (with arbitrary distributed check bit positions) for the polynomial expressing the difference between $R_{i+1}(x)$ and $xR_i(x)$ for the case where parity check bits are distributed throughout the frame becomes too impractical to derive. Instead, the specific DS3-FEC case with distributed check bits is considered. Because of the length of the code involved only the differing positions between the left shift of R_i and R_{i+1} are tabulated.

Let $Rdistr_i = (a_{1360}, a_{1359}, \ldots, a_2, a_1)$ be the block of bits in the receiver buffer at time i. The systematic form of $Rdistr_i$, R_i is obtained by rearranging the distributed check bits into the systematic positions. At time i+1, let $Rdistr_{i+1} = (a_{1359}, a_{1358}, \ldots, a_1, a_0)$ be the block of bits in the receiver buffer, and R_{i+1} be its systematic form after the rearrangement of the check bits. Let the vector Ddistr (or the polynomial Ddistr(x)) be the difference between left shift of R_i and R_{i+1}. Following an analysis similar to that done in Sec. 3.5.3, it can be shown that the relationship between the syndromes at times i+1 and i is:

$$S_{i+1}(x) = xS_i(x) \bmod g(x) + Ddistr(x) \bmod g(x) \tag{3.26}$$

where

$$Ddistr(x) = \sum_{j=1}^{25} d_j x^{p_j} \tag{3.27}$$

which accounts for the 25 differences between the left shift of R_i and R_{i+1}. d_j is the sum (modulo-2) of the appropriate pairs of bits in $Rdistr_i$;

$$d_j = a_{j1} + a_{j2} \tag{3.28}$$

Note that j1 and j2 are bit positions in $Rdistr_i$.

The values of the position indices j1 and j2 (corresponding to a_{j1} and a_{j2} used to obtain d_j), and the associated values of p_j are given in Table 3.1.

Table 3.1 Values of j1, j2, and p_j for Ddistr(x).

d_j	d_1	d_2	d_3	d_4	d_5	d_6	d_7	d_8	d_9	d_{10}	d_{11}	d_{12}	d_{13}	d_{14}	d_{15}	d_{16}	d_{17}	d_{18}	d_{19}	d_{20}	d_{21}	d_{22}	d_{23}	d_{24}	d_{25}
j1	1360	1274	1104	1019	934	849	764	594	424	339	254	169	84	1275	1105	1020	935	850	765	595	425	340	255	170	N/A
j2	N/A	1275	1105	1020	935	850	765	595	425	340	255	170	85	0	1274	1104	1019	934	849	764	594	424	339	254	169
p_j	1359	1274	1105	1021	937	853	769	600	431	347	263	179	95	11	10	9	8	7	6	5	4	3	2	1	0

Note that bit 1360 is the MSB of the receiver buffer at time i and bit 0 (used to compute d_{14}) is the newly arrived bit.

As before each of x^{p_j} mod g(x) is some fixed polynomial of degree less than n-k and can be precomputed and used in conjunction with d_j to obtain the syndrome $S_{i+1}(x)$ in a manner similar to that described earlier. The syndromes for each of x^{p_j} mod g(x), in binary form, are tabulated in Table 3.2. The schematic architecture for realizing the CCSC scheme in the distributed case is shown in Fig. 3.10.

Table 3.2 Syndromes [x^{p_j} mod g(x)] for $p_j \geq 11$.

d_j	p_j	syndrome (MSB first)
d_1	1359	01000001101
d_2	1274	00011010100
d_3	1105	01111001110
d_4	1021	11111111011
d_5	937	01010001001
d_6	853	11111100100
d_7	769	10111111011
d_8	600	11011010010
d_9	431	01110100111
d_{10}	347	10100110000
d_{11}	263	11001001011
d_{12}	179	00101011100
d_{13}	95	00010100010
d_{14}	11	00000000101

Note that the syndrome of each of x^{p_j} for $p_j < 11$, is equal to x^{p_j}.

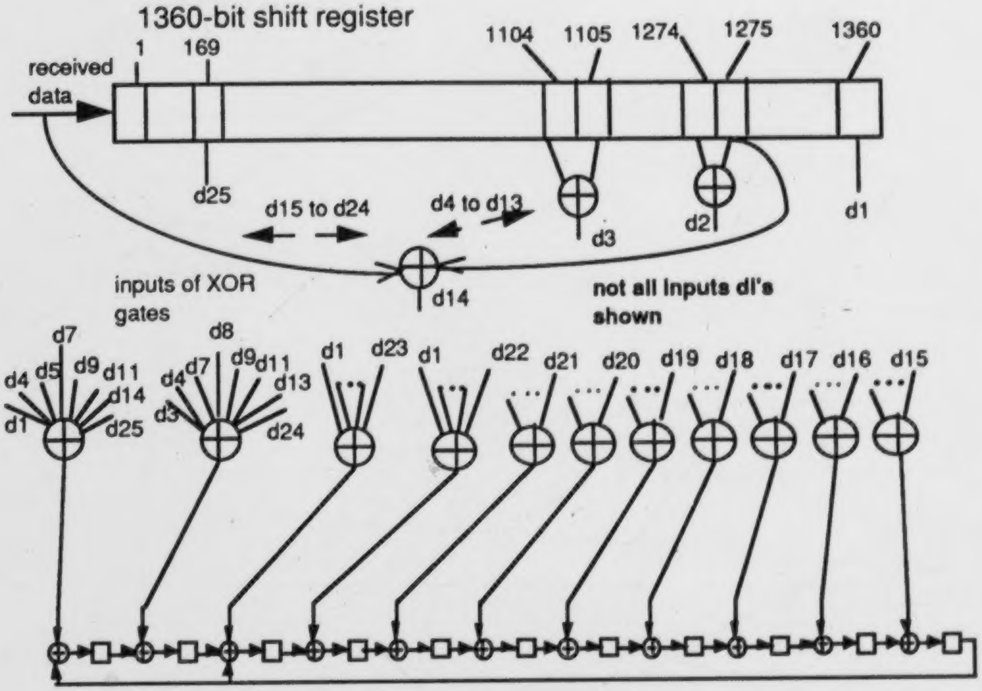
1360-bit shift register
received data
1
169
1104
1105
1274
1275
1360
d25
d15 to d24
d4 to d13
d3
d2
d1
d14
inputs of XOR gates
not all inputs di's shown
d7
d4 d5 d9 d11
d14
d1
d25
d8
d4 d7 d9 d11
d13
d3
d24
d1 d23
d1 d22
d21
d20
d19
d18
d17
d16
d15

Fig. 3.10. CCSC scheme for the DS3-FEC code.

The number of differing positions tabulated in Table 3.1 is 25 which is greater than n-k. Therefore, similarly as in the systematic reversed code, it can be shown that p_m in this case is always equal to 2^{k-n}. In addition, for extended codes, if the overall even parity check bits are also used for framing, the value of p_m will be further reduced by a factor of 2. The values of p_m as a function of d obtained using computer simulations are plotted in Fig. 3.11. It is found that the value of p_m deviates negligibly from its theoretical value 2^{-12} for all values of d. The average value of p_m obtained by simulation is 0.000247, which is only marginally larger than 2^{-12} (0.000244).

The CCSC schemes for the four cases above require an initial correct computation of a syndrome for the first word in the receiver buffer. This can be easily achieved during start-up and reset periods when both the content of the receiver buffer and the syndrome register are set to zero.

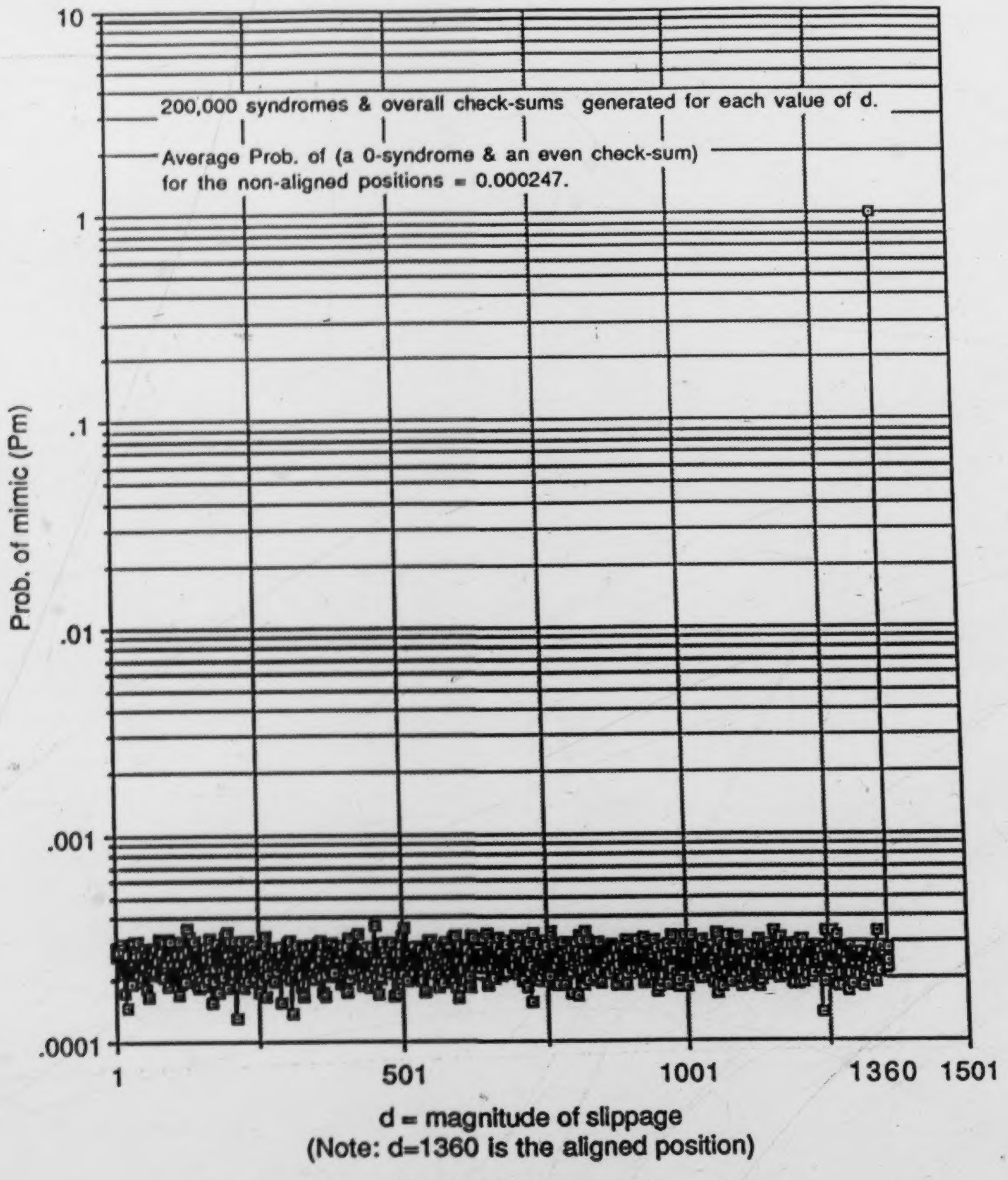

Fig. 3.11 Prob. of mimic vs d (magnitude of slippage) for the DS3-FEC (distributed) code .

3.5.5 The Decoding Function of CCSC

Note the CCSC for the four cases analyzed all have the capability of evaluating a syndrome every bit time. The CCSC is used by the search process during the reframing phase to validate whether a position is the frame aligned position. During the in-frame state, the CCSC continues to compute a syndrome every bit time, but the decoder only uses the syndrome at every frame period to perform error location and correction functions. Syndromes obtained not at frame period times are not used and only serve as intermediate syndromes from which the syndromes at the frame intervals are obtained. Note that the CCSC circuit computes syndromes from frame to frame and the content of its syndrome register is never reset at all (this is in contrast to a normal decoder circuit which resets the content of syndrome register to zero at the start of every frame or code word period). This is because the computation of a syndrome at a given bit time, in the CCSC scheme, is obtained by modifying that obtained the previous bit time. Note also that the presence of errors in the received FEC frames does not affect the CCSC; because the CCSC circuit simply does the continuous computation for the block of bits going (shifting) through the receiver buffer regardless of their contents.

As far as computing the syndrome for the decoding (SEC-DED) operations, the CCSC circuit is slightly more rapid than the syndrome circuits employed in a normal decoder. To decode the distributed DS3 code (with distributed parity check bits) a conventional decoder would compute the syndrome in two steps. First, it would shift all the data (non parity check) bits through the syndrome circuit while the parity check bits at the 12 distributed positions are collected. When all the data bits have been shifted through (which requires 1360 bit times), the collected parity check bits are shifted through to produce the final syndrome. Decoding of this type is exhibited in [2] and [3]. The two steps syndrome computation process required a total of 1360+12 bit times (longer than the frame period). This means the syndrome circuit is not available at the start of the next frame period to compute the syndrome for the next received frame. Therefore, a second syndrome circuit is needed and together the two circuits work in a staggered way (i.e. their control timing is offset from each other by 1 frame period) and each computes the syndromes for alternate received frames. The disadvantages of a normal decoder syndrome computation for the distributed code are:

i. twelve bit times more delay for decoding.

ii. one additional syndrome circuit is required.

iii additional circuitry for the timing and control of the staggered syndrome circuits.

iv. circuitry for the timing and control of the selective collections of parity check bits.

In contrast, the CCSC completes the syndrome computation for each frame in 1360 bit times. Only one CCSC circuit, (except that it is more complex than a normal syndrome circuit because it involves 25 two-input and 11 multiple-input additional exclusive-or gates, and also 11 1-bit delay elements), is sufficient and the selective collections of the twelve distributed parity check bits are not needed, hence less overall timing and control circuitry may be required. In practice the comparison of implementation complexity between the two schemes is not straight forward, as it depends on the type of silicon implementation process used. Moreover the CCSC circuit has a dual function, here, of facilitating framing and error control.

3.5.6 Relative Framing Search Speed with Each CCSC Method

If no mimics occur (or no zero syndrome is ever computed at an non-aligned position), the reframing circuit (using the CCSC scheme) can complete the rejection process of each non-aligned position in only one bit time. However, in practice zero syndromes can be computed (mimics) at non aligned positions due to mimicking of a valid code word by misaligned data. The occurrence of a mimic prolongs the rejection process by at least one frame time because any zero syndrome requires that we dwell on the corresponding frame boundaries to determine if zero syndromes repeatedly arise at these boundaries. Longer search times are therefore expected for schemes which have a higher probability of mimic. For this reason, systems using distributed or systematic reversed code (which have the lowest possible value of p_m) will cause shorter search times (hence reframe times) than those systems using shortened and extended systematic codes. The longest search times are expected for systems using full length systematic codes. The p_m values as high as 1/2 and 1/4 for systematic codes also mean larger reframe confirmation threshold values are required to eliminate false in-frame declarations.

3.6 The Reframing and Out-of-frame Detection Architectures

3.6.1 The Reframing Circuit

The schematic of the reframing (RF) circuit for the DS3-FEC code is shown in Fig. 3.12. The functionality of this circuit is as follows:

i. The reframing circuit is activated (enabled) whenever an OOF state has been declared.

ii. It examines the decoded syndromes of the CCSC circuit and the overall check-sums every bit time in order to check for the occurrence of a valid code word.

iii. When no valid code word has been decoded, slip signals are generated every bit time to introduce slips (one bit time shifts) to the start of the FEC frame clock.

iv. When a valid code word has been decoded, the slip signals are disabled and the reframe (RF) counter is incremented by 1. The confirmation process is started and subsequent checks for a valid code word (and updates of the RF counter) are only done at the end of every frame period determined by the current FEC frame timing.

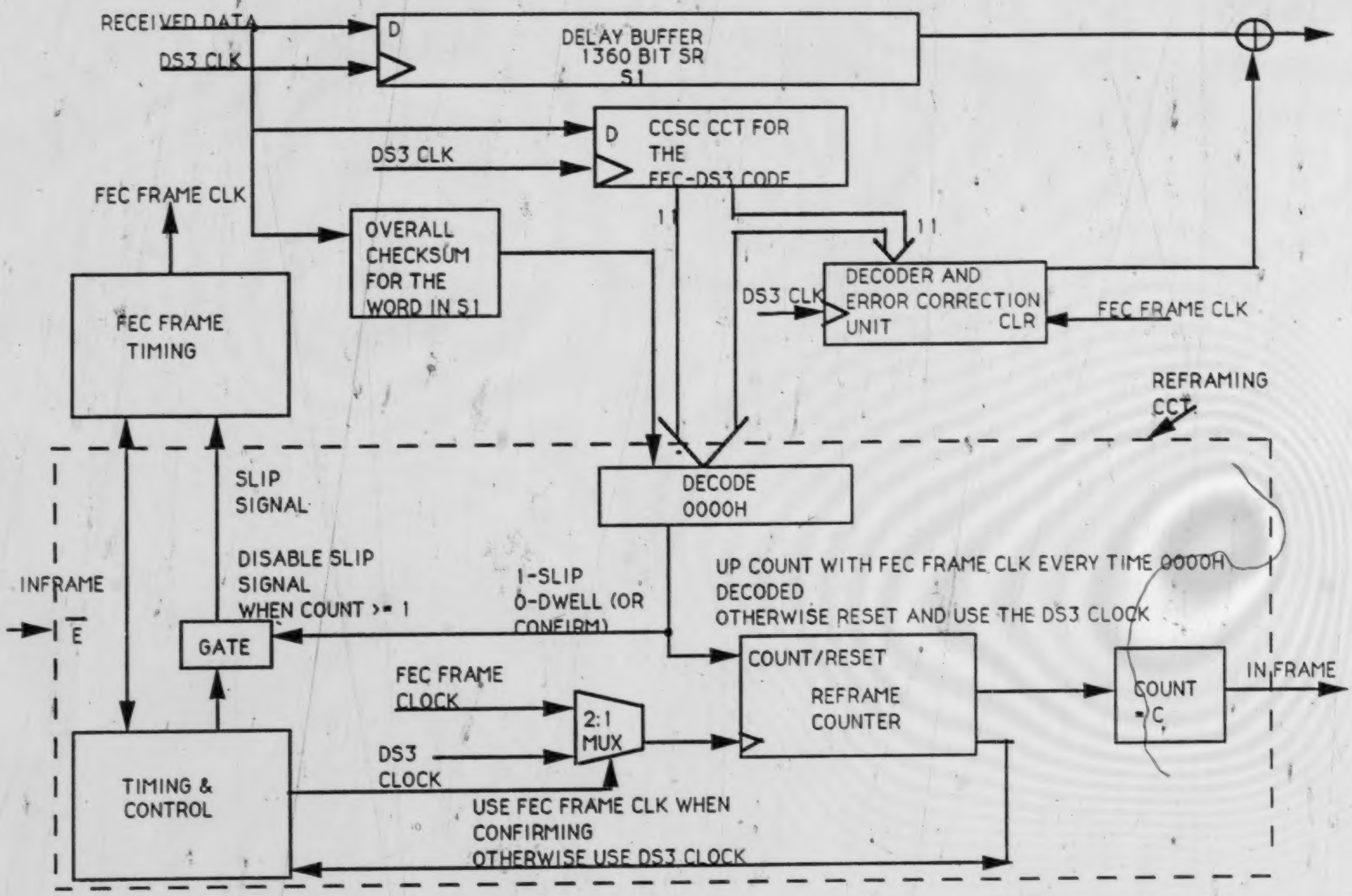
RECEIVED DATA
DS3 CLK
D
DELAY BUFFER
1360 BIT SR
S1
D
CCSC CCT FOR
THE
FEC-DS3 CODE
DS3 CLK
FEC FRAME CLK
OVERALL
CHECKSUM
FOR THE
WORD IN S1
11
11
DECODER AND
ERROR CORRECTION
UNIT
CLR
DS3 CLK
FEC FRAME CLK
FEC FRAME
TIMING
REFRAMING
CCT
SLIP
SIGNAL
DECODE
0000H
DISABLE SLIP
SIGNAL
WHEN COUNT >= 1
1-SLIP
0-DWELL (OR
CONFIRM)
UP COUNT WITH FEC FRAME CLK EVERY TIME 0000H
DECODED
OTHERWISE RESET AND USE THE DS3 CLOCK
INFRAME
E
GATE
COUNT/RESET
REFRAME
COUNTER
COUNT
= C
IN FRAME
FEC FRAME
CLOCK
2:1
MUX
DS3
CLOCK
TIMING &
CONTROL
USE FEC FRAME CLK WHEN
CONFIRMING
OTHERWISE USE DS3 CLOCK

Fig. 3.12 Block diagram of the reframing circuit.

v. When an invalid code word has been decoded during the confirmation the RF counter is reset back to zero and the process described in iii. is repeated.

vi. When the RF counter reaches the reframe confirmation threshold value the IN-FRAME signal is generated and the reframing circuit is disabled.

3.6.2 The Out-of-frame Detection Circuit

The schematic architecture of the out-of-frame detection (OFD) circuit for the DS3-FEC code is shown in Fig. 3.13. The functionality of this circuit is as follows:

i. The OFD circuit is enabled during the in-frame state.

ii. The validity of each received word (stored in the delay buffer) is checked by examining the syndromes computed by the CCSC circuit and the overall check-sum at the end of every FEC frame period.

iii. A decoded invalid code word increments the OFD counter by a value of 1 and a decoded valid code word resets the OFD counter to zero.

iv. When the OFD counter reaches the OFD confirmation threshold the OOF signal ($\overline{\text{IN-FRAME}}$) is generated which also activates the reframing circuit to perform a reframe.

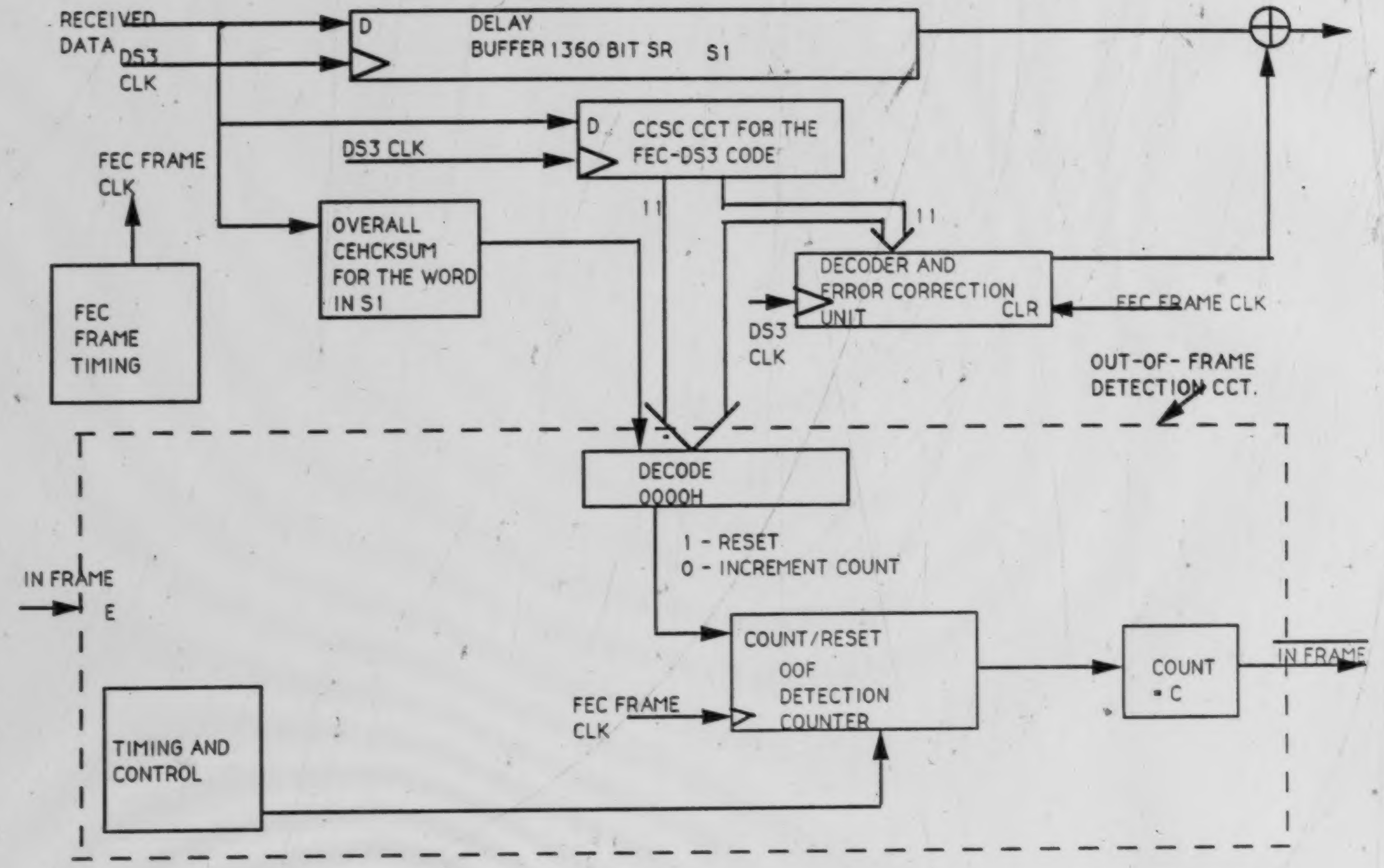
RECEIVED DATA
DS3 CLK
D
DELAY BUFFER 1360 BIT SR S1
D
CCSC CCT FOR THE FEC-DS3 CODE
DS3 CLK
FEC FRAME CLK
OVERALL CEHCKSUM FOR THE WORD IN S1
FEC FRAME TIMING
11
11
DECODER AND ERROR CORRECTION UNIT
CLR
FEC FRAME CLK
DS3 CLK
OUT-OF- FRAME DETECTION CCT.
DECODE 0000H
1 - RESET
0 - INCREMENT COUNT
IN FRAME
E
COUNT/RESET OOF DETECTION COUNTER
FEC FRAME CLK
COUNT = C
IN FRAME
TIMING AND CONTROL

Fig. 3.13 Block diagram of the out-of-frame detection circuit.

3.7 Computer Simulation Techniques

Computer procedures have been developed to simulate the following operations and parameters:

i. Encoding and decoding -

A procedure has been developed to emulate the encoding operations (described in Sec. 3.2 and Fig. 3.1) and the decoding operations (specifically the CCSC method described in Sec.3.3 and Fig. 3.3 and Fig. 3.10) of the DS3-FEC code. The data bits for the DS3 code words are generated using a random number generator. The bits in the encoded code words are serially transferred (stored) into the "receiver buffer" of the decoder routine and the decoder routine always keeps track of the true frame alignment timing.

ii. Probability of mimic -

The encoding and decoding routines of i. are run continuously for the desired number of frames. The number of zero syndromes decoded for each misaligned bit position (relative to the frame boundaries) is recorded for the computation of the probability of mimic associated with this bit position.

iii. Reframe time -

A computer procedure has been developed to emulate the reframing operations (described in Sec. 3.6 and Fig. 3.12). It also employs the encoding and decoding routines developed for i. To obtain the maximum (length) reframe time statistics, each reframe operation is initiated at just one bit after the true frame alignment bit position. The time it takes to complete each reframe is recorded. To simulate the reframes in an environment having line errors a random number generator is used to randomly insert errors, at the desired BER, into the encoded words before they are transferred to the "receiver buffer" of the decoding routine.

iv. Out-of-frame detection time -

A computer procedure has been developed to emulate the out-of-frame detection (OFD) operations described in Sec. 3.6 and Fig. 3.13. An OOF condition is created by introducing timing (bit position) errors in the frame alignment timing. The time taken to actually detect the OOF condition is recorded. Repeated simulations of the OOF detections are done to obtain long term statistics for the OFD times.

Because the computer simulations involved in this work are emulations of actual logic operations (which involve shifting and exclusive-or operations on bits in the involved shift registers), the results obtained from the simulations are considered as (computer) experimental results.

Complete source listings (and documentations) for all of the simulations used in this thesis are given in [15].

3.8 Timing Parameters of FEC Framing

The framing circuit's behaviour in FEC framing is analogous to that of conventional frame alignment word (FAW) or burst framing, except that in the FEC case syndromes are examined, whereas in the conventional case FAB's are examined. Checking for a zero syndrome in the FEC case is just like checking for an FAW with an all-zero pattern. Therefore, the behaviour of FEC framing can be analyzed in the same way as the framing with a FAW (burst). Also the behaviour of FAB and FAW framing are identical except in the FAB framing individual bits are examined whereas in the case of FAW framing words are examined. Using this fact, the timing parameters of FEC framing are analyzed as follows.

3.8.1 Maximum Reframe (MRF) Time

i. The search process

The search process of FEC framing is depicted in Fig. 3.14. It is identical to that of Fig.2.3 except the probability p_s of an F-bit simulation is replaced by the probability of a code word mimic p_m. A slip in this case requires only δ (1 bit) time (because a new syndrome is examined every bit time). The signal transfer function from state i to i+1 is given by:

$$\frac{q_m z^{\delta}}{1 - p_m z} \tag{3.29}$$

where, for the DS3-FEC code, $p_m = 2^{-12}$ is the probability of a misaligned word mimicking a valid code word (i.e. a misaligned word having a zero syndrome and an even overall parity check sum), and $q_m = 1- p_m$. $\delta = 1/n = 1/1360$ is the normalized duration of a single bit in the DS3-FEC frame.

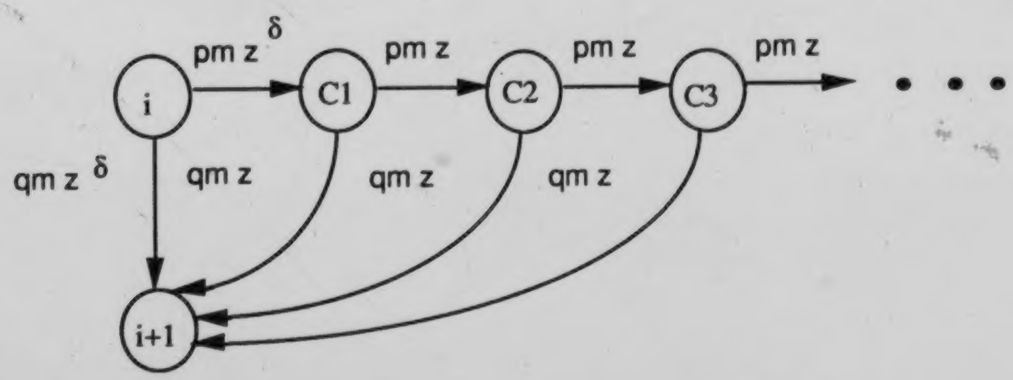

Fig. 3.14 Falsehood detection process for 1 bit.

The signal transfer function for a maximum length search (involving the rejection of *n-1* bits) is:

$$\tau(z) = \left(\frac{q_m z^{\delta}}{1 - p_m z}\right)^{n-1} z^{\delta} \tag{3.30}$$

ii. The combined search and confirmation process

The confirmation process for FEC framing is identical to that of FAB framing (see Fig. 2.3) except that the successful detection of the code word only occurs when no error has corrupted the 1360 bits frame. Therefore the probability of a successful detection p_d per frame is given by:

$$p_d = (1 - p_e)^{1360} \tag{3.31}$$

where p_e is the channel BER.

The signal transfer function for the overall maximum length reframe process is (the same as that specified in equation (2.5)):

$$P_{RF}(z) = \frac{p_d^c \, \tau(z) \, z^{c-1}}{1 - q_d \, \tau(z) \dfrac{1 - p_d^c \, z^c}{1 - p_d \, z}} \tag{3.32}$$

where, $q_d = 1 - p_d$.

3.8.2 False in-Frame (FF) Time:

The false in-frame declaration procedure is depicted in Fig. 3.15. Once again it is identical to that of FAB framing except that each slip requires only δ (1 bit) time and the probability p_s, of an F-bit simulation is replaced by the probability of mimic, p_m, of a valid code word. The signal transfer function for the false in-frame process is:

$$P_{FF}(z) = \frac{p_m^c \, z^{c+\delta+1}}{1 - q_m \, z^{\delta} \dfrac{1 - p_m^c \, z^c}{1 - p_m \, z}} \tag{3.33}$$

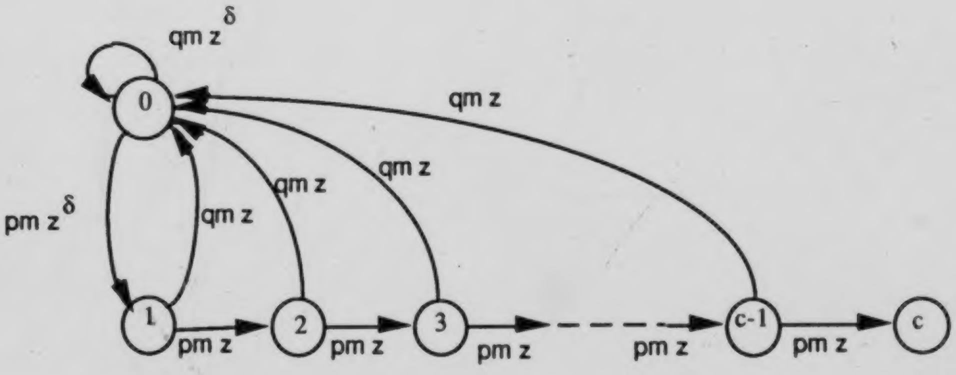

Fig. 3.15 False-in-frame declaration procedure (FEC).

3.8.3 Out-of-frame Detection (OFD) and Misframe (MF) Times:

Misframes occur when multiple FAB's (or FAW's) are corrupted by channel errors. In the FAB case the probability of FAB corruption is equal to p_e (or $BER_{channel}$), whereas in the FEC case, the probability of a non-zero syndrome is approximately equal to 1360 p_e. Therefore for the same OOF confirmation threshold value, misframes are more likely to occur in FEC framing. To have a better misframe performance larger values of the confirmation threshold for the FEC case should be chosen. As for the choice of the out-of-frame detection criterion, the "c successive count" scheme is adopted because its stricter out-of-frame declaration criterion (which gives longer misframe times) is more desirable than that of the "x-out-of-K" scheme (when c = x) with the large FEC blocks. The use of the "c successive count" criterion for FEC framing is also justified because the value of the probability of mimic (simulating a valid code word) is extremely small (= 2^{-12}) which means when an OOF condition has actually occurred it is highly probable that c successive non-zero syndromes are obtained.

The OOF detection declaration procedure for FEC framing is depicted in Fig. 3.16. The out-of-frame detection count is incremented by one each time a non-zero syndrome is obtained for a misaligned frame. When a zero-syndrome is obtained (due to a mimic of a valid code word by a misaligned word) the count is reset to zero. c successive error syndromes (non-mimics) cause the declaration of the OOF state. The signal transfer function for the OF times is:

$$P_{OF}(z) = \frac{q_m^c z^c}{1 - p_m z \frac{1 - q_m^c z^c}{1 - q_m z}} \tag{3.34}$$

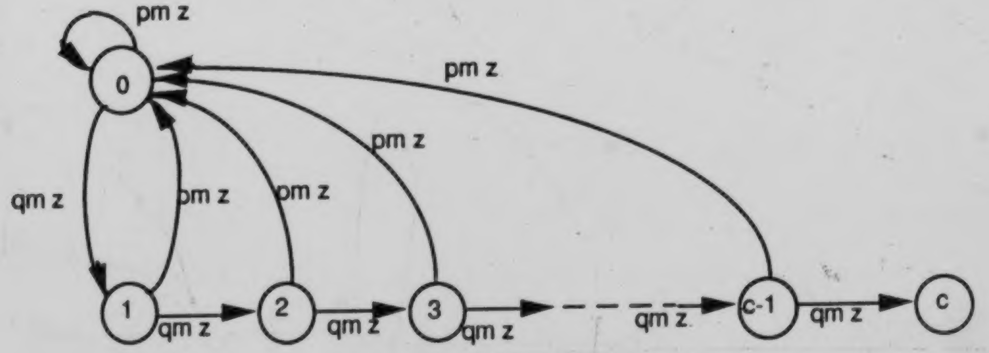

Fig. 3.16 Out-of-frame declaration procedure.

The misframe declaration procedure is shown in Fig. 3.17. The procedure is identical to that of the OOF detection declaration procedure except the probability of mimic is replaced by the probability of a successful detection of the properly aligned frame. (i.e. p_d and q_d are used instead of p_m and q_m). The signal transfer function for the MF times is:

$$P_{MF}(z) = \frac{q_d^c z^c}{1 - p_d z \frac{1 - q_d^c z^c}{1 - q_d z}} \tag{3.35}$$

where p_d, q_d are the same as those specified for equations (3.32) and (3.33).

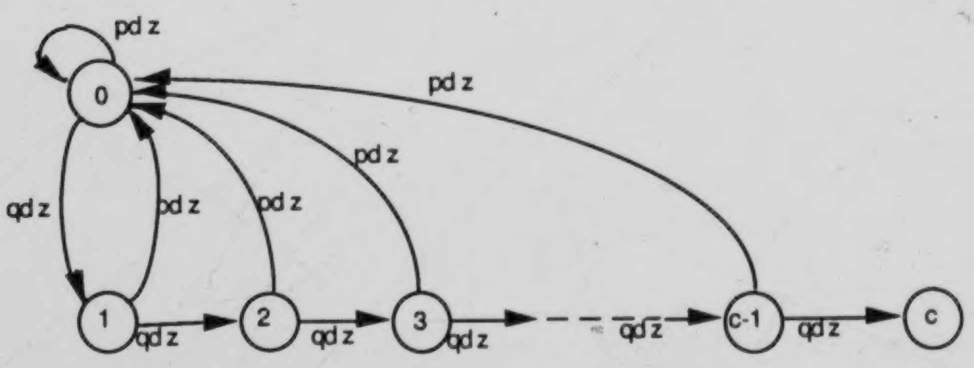

Fig. 3.17 Misframe declaration procedure.

3.9 Statistical Characterization of the Framing Parameters

The averages, standard deviations, and other percentile values (only in the MRF and OFD cases) of the four framing parameters have been computed from their PGF's for different values of the parameter c. The MRF, FF, and OFD times are given in Table 3.3. Note that the values are expressed in (normalized to) F-bit intervals so as to allow direct comparison with those obtained for conventional DS3 framing. The corresponding MRF and OFD values obtained experimentally are shown in Table 3.4. The experimental values are consistent with the values in Table 3.3.

Table 3.3 Framing parameters for FEC framing.

	Mean	Standard Deviation	99.5 percentile	99.8 percentile	99.9 percentile
MRF[1] (c=2)	18.7	4.68	40	40	48
MRF[2] (c=3)	26.7	4.78	48	48	56
FF(c=2)	$1.31*10^5$	$1.31*10^5$	N/A	N/A	N/A
FF(c=3)	$5.38*10^8$	$5.38*10^8$	N/A	N/A	N/A
OFD(c=5)	40.029	0.928	40	40	48
OFD(c=6)	48.041	1.193	48	48	64

---

[1] The values for MRF(c=2) are for BER = 10^{-6}; for BER's ranging from 10^{-4} to 10^{-10}, the mean values range from 23.15 to 18.66 quarter frames.

[2] The values for MRF(c=3) are for BER = 10^{-6}; for BER's ranging from 10^{-4} to 10^{-10}, the mean values range from 35.6 to 26.66 quarter frames.

P_F (c=2,BER = 10^{-6}) = 8.12 * 10^{-5}, P_F (c=3, BER = 10^{-6}) = 1.99 * 10^{-8}; P_F is obtained using (2.9).

Table 3.4 Experimental framing parameters for FEC framing.

	Mean	Standard Deviation	99.5 percentile	99.8 percentile	99.9 percentile
MRF (c=3)	26.76	4.83	48	48	56
OF(c=6)	48.040	1.184	48	48	64

The probability distributions of the MRF and OF times are obtained by expanding their respective PGF's and are plotted in Fig. 3.18 and 3.19 respectively. The probability distributions of the MRF times for BER = 10^{-6} obtained experimentally and analytically are compared in Fig. 3.20. The comparison shows very good agreement.

The values of the average misframe time T_{MF} (or their logarithms), in units of F-bit intervals and in actual time, for BER ranging from 10^{-4} to 10^{-10} are shown in Table 3.5.

Table 3.5 Misframe times of FEC framing.

Log(BER)	-4	-5	-6	-7	-8	-9	-10
(c=5) Log(T_{MF})	5.4	10.3	15.2	20.2	25.2	30.2	35.2
Time	0.95 secs	21 hrs	190 yrs	1.9 10^{7} yrs	1.9 10^{12} yrs	1.9 10^{17} yrs	1.9 10^{22} yrs
(c=6) Log(T_{MF})	6.3	12.1	18.1	24.1	30.1	36.1	42.1
Time	8 secs	1.8 mths	1.5 10^{5} yrs	1.5 10^{11} yrs	1.5 10^{17} yrs	1.5 10^{23} yrs	1.5 10^{29} yrs

The misframe times are compared with those of F-bit framing in Fig. 3.21.

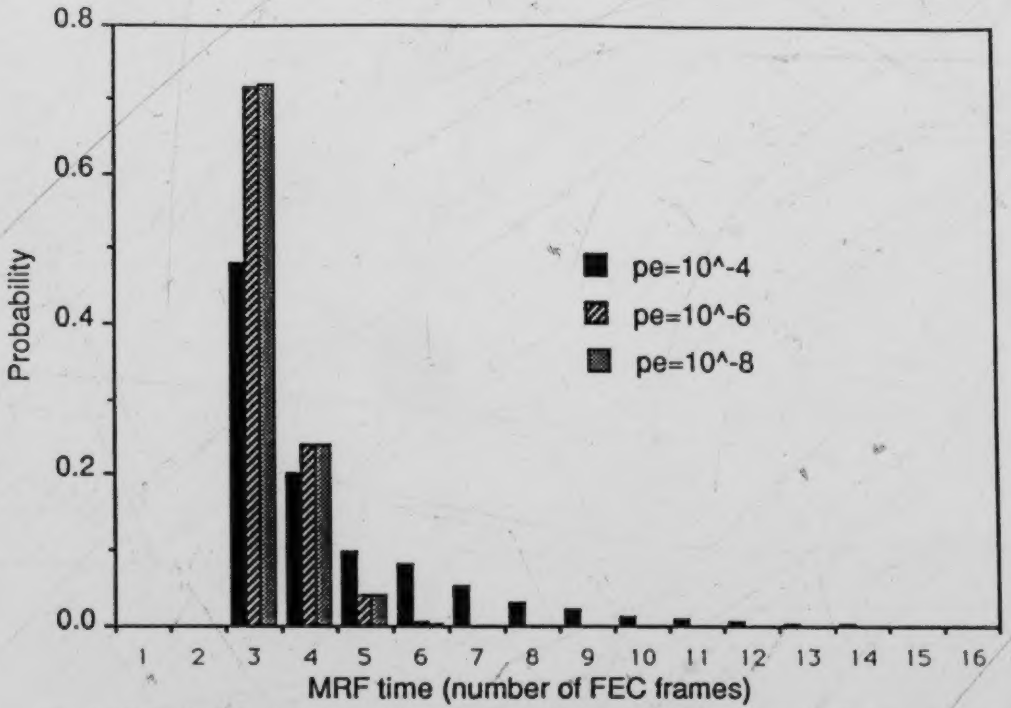

Fig. 3.18 Probability distributions of MRF times of FEC framing (c=3) for various pe's.

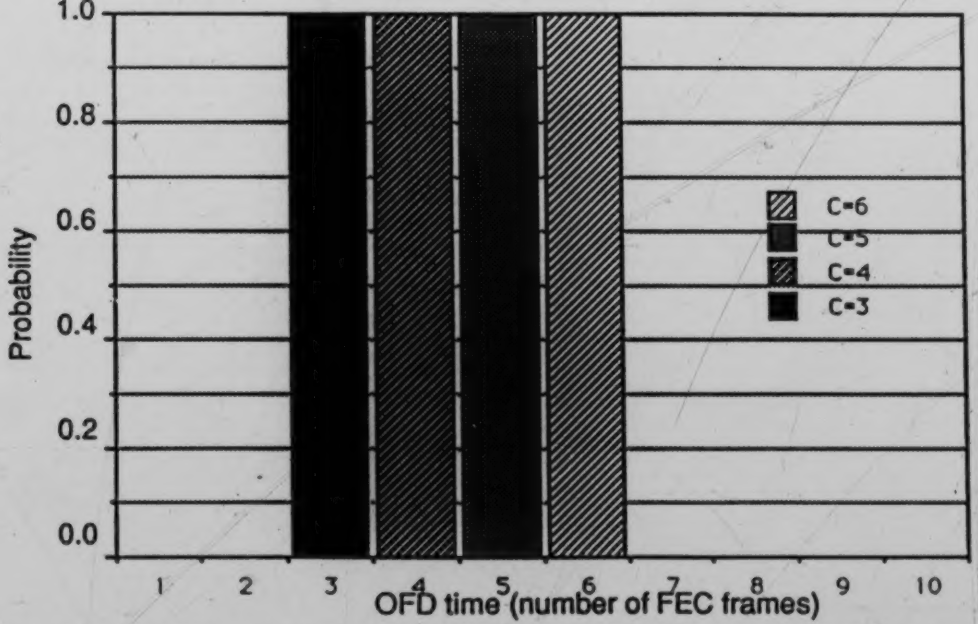

Fig. 3.19 Probability distributions of the OFD times for the (basic) FEC OOF detections.

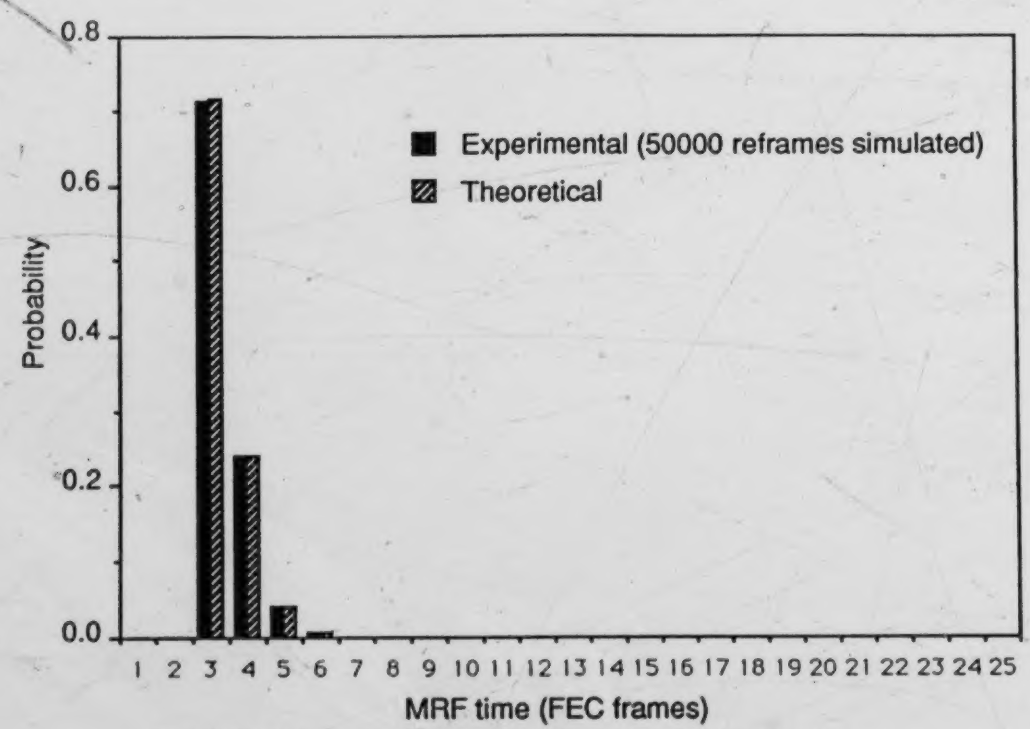

Fig. 3.20 Comparison of the experimental and theoretical probability distributions of MRF times of FEC framing (c=3, pe=10^-6)

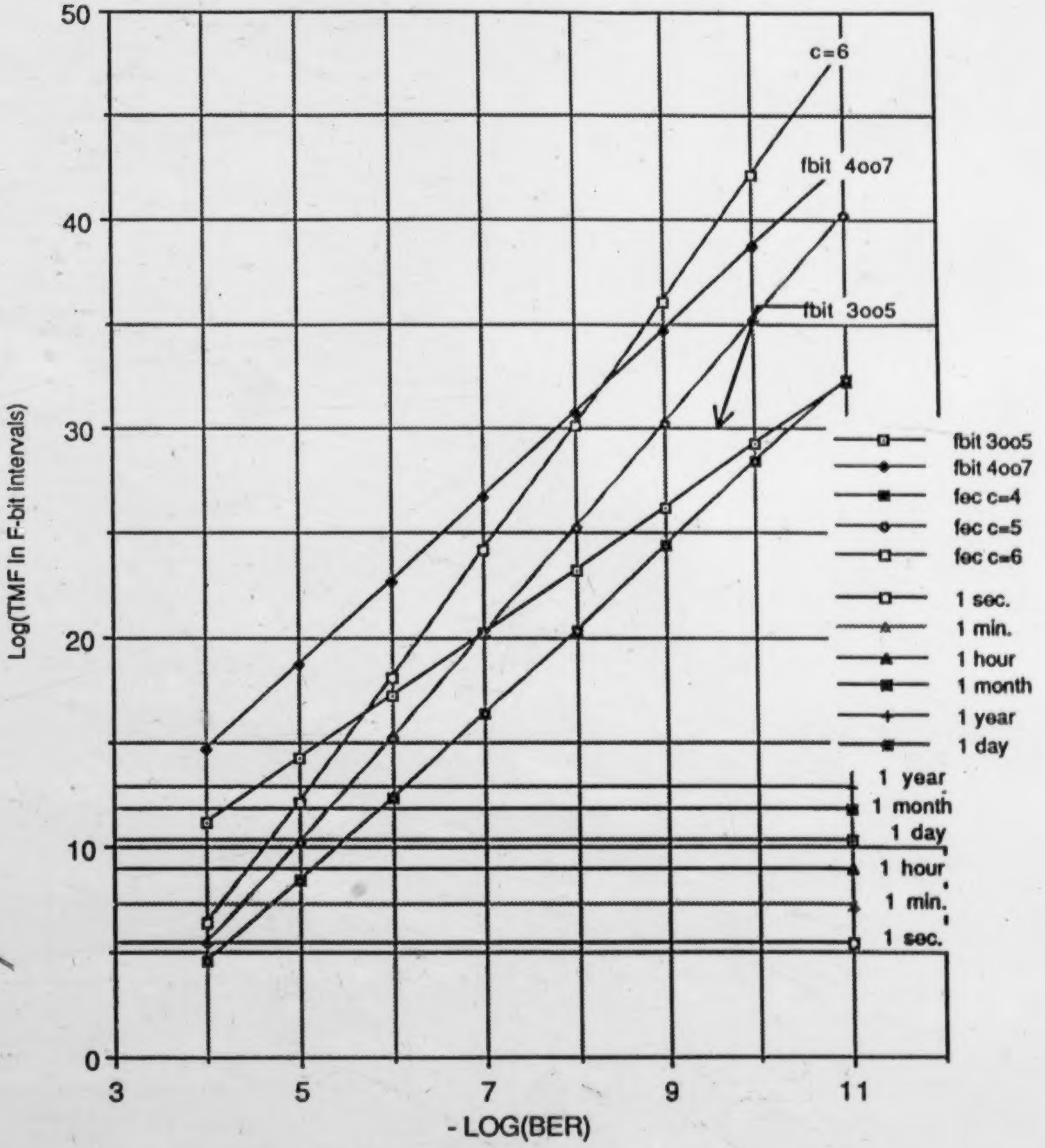

Fig. 3.21 Comparison of TMF's for F-bit and Basic FEC OFD schemes.

3.10 Selection of the Reframe and Out-of-frame Detection Confirmation Thresholds

The reframe confirmation threshold c has been chosen as 3 because values lower than 3 do not give long enough T_{FF}. The OOF detection confirmation threshold has been chosen as 6 because values lower than 6 would not guarantee long enough T_{MF} for degraded BER (such as 10^{-5}). At usual BER's of below 10^{-8}, misframes practically never happen.

3.11 BER of the FEC Protected DS3 Data.

The DS3-FEC (SEC-DED) code has the following error control functions:

i. corrects any single error occurring in a frame.

ii. detects any double (or even number of) errors occurring in a frame.

iii. adds at most one error to any multiple odd errored frame.

Because the presence of multiple odd number of errors (in a frame) is treated by the decoder as if a single error has occurred, an error correction attempt is made inadvertently if the location specified by the decoded syndrome is a data bit position. This is known as error extension. Error extension is possible for all frames that have multiple odd number of errors. For BER levels ($< 10^{-7}$) characteristic of DS3 transmission channels, the probability of having 5 or more errors in a frame is very small ($\cong 1/10^{22}$). Therefore error extensions due to their occurrences can be neglected, and let us consider only the effect of error extensions for frames with 3 errors.

Error extension does not result when the correction location specified by the syndrome (decoded for frames with multiple odd errors) points to a position other than the data bit positions of the frame. For shortened codes this includes all the parity check bits, and the non-existent leading bit positions present in the parent code. Therefore, the expected value of the number of errors denoted by N_e[1] when three errors have occurred is given by:

$$N_e = (4\frac{k}{n_p} + 3\,\frac{n_p - k}{n_p}) \tag{3.36}$$

where k = 1348 is the number of data bits, $n_p = 2047$ is the length of the parent code.

Consequently, when neglecting the effect due to 5 or more errors (in a frame), the output BER of the DS3-FEC signal becomes:

$$BER_{output} = \frac{1}{k}[2(nC_2)\, p_e^2\, q_e^{1358} + N_e\,(nC_3)\, p_e^3\, q_e^{1357} + 4\,(nC_4)\, p_e^4\, q_e^{1356}] \tag{3.37}$$

where nC_k is the number of combinations for choosing k out of n items.

To first order, the pratical output BER of the system, is given by the p_e^2 term only at the channel BER levels of interest ($\leq 10^{-4}$), using the above FEC code is:

$$BER_{out} \cong 1359\,(BER_{channel})^2 \tag{3.38}$$

The output BERs with the FEC protection for various input BERs are plotted in Fig. 3.22.

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[1] Simulation has empirically determined that the attempted correction location in cases of multiple errors can be approximated as a random variable uniformly distributed over the span of the original parent code.

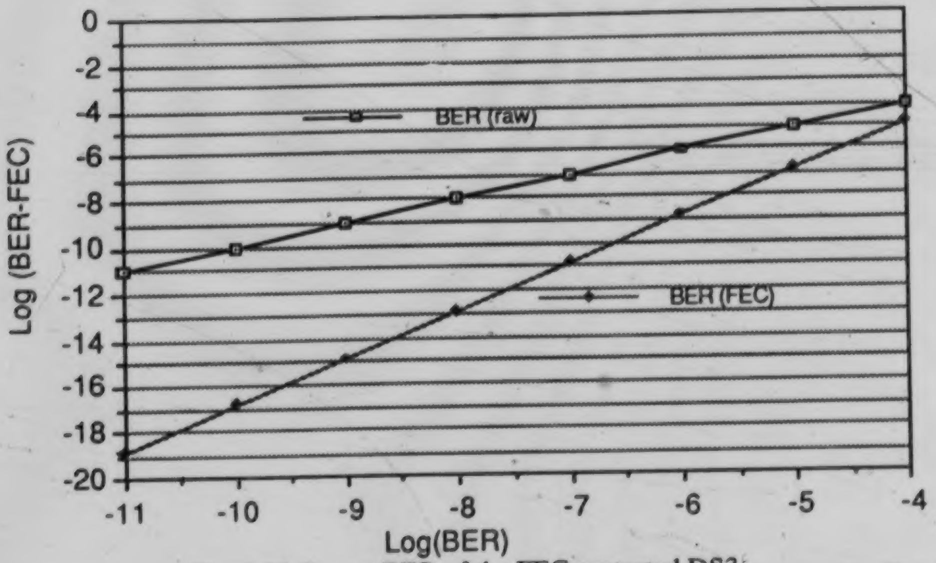


Fig. 3.22 Output BER of the FEC protected DS3.

3.12 FEC Performance for an Example Commercial DS3 Circuit

A twenty two day log of continuous error-second data for a actual commercial DS3 circuit was obtained from a telephone company. The error count chart which depicts the number of errors occurring in each minute of the 22 days is shown in Appendix C. It is found that in the logged period, there are a total of;

i. 1156 single-errored seconds,

ii. 15 double-errored seconds,

iii. 1 triple-errored second.

The number of errors together with the average interval-BER for the worst second, worst minute, worst hour, and worst half day (12 hours), together with the overall BER of the 22 days period are tabulated in Table 3.6.

Table 3.6 Number of errors and BER for various intervals of the analyzed DS3 circuit.

	Number of errors	BER
Worst Second	3	$6.7 * 10^{-8}$
Worst Minute	15, includes one double-errored second	$5.6 * 10^{-9}$
Worst Hour	88, includes 2 double-errored seconds	$5.5 * 10^{-10}$
Worst 12 Hour	252, includes 2 double-errored seconds	$1.3 * 10^{-10}$
Average BER Over 22 Days Observation	1189, includes 15 double-errored seconds and 1 triple-errored second	$1.4 * 10^{-11}$

If the proposed DS3-FEC code had been implemented it would have corrected every one of the errors occurring in the 1156 single errored seconds. For double (or triple) errored seconds, there is no information indicating whether the double (or triple) errors occurred simultaneously in one of 32,894 FEC frames in the errored second. Therefore, it is assumed that errors occurring in multiple errored seconds are independently distributed and with this assumption the following probabilities are derived:

The probability of the 2 errors in a double errored second occurring in the same FEC frame (i.e., the probability that the 2 errors cannot be corrected) is:

$$P_A = \frac{1}{n_b \text{ (\# of FEC frames/sec.)}} = \frac{1}{32894} \tag{3.39}$$

The probability that any 2 of the 3 errors in a triple errored second occurring in the same FEC frame is (i.e., the probability that the 2 of the 3 errors cannot be corrected):

$$P_B = \frac{3}{n_b} = \frac{1}{10965} \tag{3.40}$$

The probability that 3 errors in a triple errored second occurring in the same FEC frame (or the probability that the 3 errors cannot be corrected and the error extension effect described previously applies in this case) is:

$$P_C = \frac{1}{n_b^2} = 9.242\ 10^{-10} \tag{3.41}$$

Using the probabilities P_A, P_B, and P_C the resultant BER with the FEC protection for the intervals tabulated in Table 3.5 are derived as follows:

i. the worst second:

the expected number of errors remaining uncorrected = $N_e\ P_C + 2\ P_B$; and the corresponding interval-BER = $(N_e\ P_C + 2\ P_B)$/ number of bits in a second.

ii. the worst minute:

all the errors in the 13 single-errored seconds would have been corrected, with the one remaining double-errored second, the expected number of errors remaining uncorrected = $2\ P_A$; and the corresponding interval-BER = $(2\ P_A)$/ number of bits in a minute.

iii. the worst hour:

all the errors in the 84 single-errored seconds would have been corrected, with the two remaining double-errored seconds, the expected number of errors remaining uncorrected = $2*2\ P_A$; and the corresponding interval-BER = $(4\ P_A)$/ number of bits in an hour.

iv. the worst 12 hour interval:

all the errors in the 248 single-errored seconds would have been corrected, with the two remaining double-errored seconds, the expected number of errors remaining uncorrected = $4\ P_A$; and the corresponding interval-BER = $(4\ P_A)$/ number of bits in 12 hour.

v. the 22 days logged period (overall);

all the errors in the 1156 single-errored seconds would have been corrected, with the 15 remaining double-errored seconds and one triple-errored second, the expected number of errors remaining uncorrected = $(3\ P_C + 2\ P_B + 15\ P_A)$; and the corresponding overall BER = $(3\ P_C + 2\ P_B + 15\ P_A)$/ duration of the logged period.

From the above calculations, the BER with the FEC protection for various analyzed intervals are tabulated as follows:

Table 3.7 The output BER with FEC protection for various interval of the DS3 circuit.

	BER	BER (with FEC)
Worst Second	$6.7 * 10^{-8}$	$4.08 * 10^{-12}$
Worst Minute	$5.6 * 10^{-9}$	$2.27 * 10^{-14}$
Worst Hour	$5.5 * 10^{-10}$	$7.55 * 10^{-16}$
Worst 12 Hour	$1.3 * 10^{-10}$	$6.29 * 10^{-17}$
Average BER Over 22 Days Observation	$1.4 * 10^{-11}$	$7.67 * 10^{-18}$

Therefore if the FEC code had been implemented, the burstiest BER level of $6.7*10^{-8}$ would have been reduced to $6.1 * 10^{-12}$. For other less bursty intervals the BER level would have been reduced by a factor of around 10^6. The overall BER would have been reduced from $1.4 * 10^{-11}$ to $7.6 * 10^{-18}$. These results are very significant as they show that in the practical environment of modern FOTS-borne DS3 transport the proposed scheme would be quite effective.

4. IMPROVED OOF DETECTION SCHEMES FOR FEC FRAMING

The OFD times of the OOF detection scheme for FEC framing which is based on the validity of the examined code word are much longer than those of F-bit framing. The relatively long OFD times can be reduced (improved) by using other additional information for out-of-frame detection. The extra information available is as follows:

i) the overall parity bit# and the triple error detection information.

ii) the framing bits of the master framing structure.

Two new OOF detection schemes are derived. They are:

i) OOF detection based on the examination of decoded syndrome, overall check-sum, and the triple error detection signal every frame period.

ii) OOF detection based on the examination of the decoded syndrome, overall check-sum, the triple error detection signal every frame period (as done in i.), and also the periodic occurrences of the M, P, X bits of the master frame structure information.

We call the first scheme the "Shortened Code OOF detection" or "SC OFD" method, because triple error detections are only possible for shortened codes. The second scheme is called the "Hybrid OOF detection" or "Hybrid OFD" method, because the OOF detection is based on the combined use of the syndromes and master framing bits.

As any given OOF detection scheme not only determines the OOF detection time but also the resulting misframe (caused by channel errors) times, to maximize the misframe times the amount of increment to the OOF detection (OFD) count should be consistent with (or proportional to) the most probable number of bit errors that can be interpreted by the error detection circuit every frame period. This way of incrementing the OFD count ensures

---

# The overall parity bit has been used previously in the FEC OFD schemes to determine the validity of the examined words. Here its DED capability is used by the OFD scheme to accelerate the OFD process.

that the probability of having a particular increment, say n (due to n errors in the frame), is similar in magnitude to the nth power of the probability of having a unit increment (due to 1 error in the frame). That is $O[\text{Prob(n errors in frame)}] \cong O[\{\text{Prob(1 error in frame)}\}^{n}]$. Note also that the increment due to an error in a specific bit is 2, because the $O[\text{Prob(error in a specific bit)}] \cong O[\{\text{Prob(1 error in frame)}\}^{2}]$ for the BER levels between 10^{-6} to 10^{-8}.

To obtain the OFD and MF times for the two new schemes, the following analysis steps are required:

i. Determine the possible events that can occur at the OFD circuit, and the state transitions associated with the events.

ii. Determine the overall state transitions in the Markov model of the OFD process.

iii. From ii. construct the state transition matrices.

iv. Determine the two sets of probabilities associated with the state transitions - one set for use in the OFD declaration procedure and another for use in the misframe declaration procedure.

v. Use the appropriate set of probabilities obtained in iv. and solve the state transition matrices involved to calculate the OFD and MF times.

4.1 Shortened Code (SC) OOF Detection Scheme

In this scheme a "successive-accummulation-to-c" criterion is used. Unlike the "c-successive-count" criterion where the OFD count can only be incremented by 1 or reset back to zero with each update, for this scheme the OFD count can be incremented by a variable amount 1, 2, or 3, or reset back to zero with each update.

4.1.1 State Transitions in the Markov Model

In this scheme, the detection of either 1, 2 or 3 errors in a frame, and corresponding increase of the OFD count by a value of 1, 2 or 3 is possible by using the information in the FEC syndrome, overall check-sum and the triple error detection signal. The detection of single or double errors occurring in the frame is easily done by examining both the FEC syndrome and the overall check-sum (i.e. employing the SEC and DED capabilities of the code). The detection of certain combinations of 3 errors in the frame can be achieved by checking for the triple error detection signal at the end of a frame period.

The association of the number of errors with a decoding event is based on the following rules characteristic of SEC-DED shortened codes:

i. a zero decoded syndrome and an even overall check-sum occur when there is no error or there are some combinations of 4 errors in the frame.

ii. a zero syndrome and an odd overall check-sum are decoded when some combinations of 3 errors have occurred in the frame, or when the overall parity bit is in error.

iii. a non-zero syndrome and an odd overall check-sum are decoded, when 1 error or some combinations of 3 errors occur in the frame.

iv. a non-zero syndrome and an even overall check-sum are decoded, when 2 or some combinations of 4 errors occur in the frame.

v. the triple error detection signal is high at the end of a second frame period when there are some combinations of triple errors in a first frame period.

vi. the probability of 5 or more errors in a frame is less than $1/10^{22}$, and therefore these error events are neglected.

The most probable and the next most probable numbers of errors that can be interpreted from various decoder events are shown in Table 4.1. The corresponding increment to the OFD count is tabulated in Table 4.2.

Table 4.1 Number of errors associated with various decoder events.

number of errors in the frame	synd = 0	synd = 1
check-sum=0	0 or some combinations of 4 errors	2 or some combinations of 4 errors
check-sum=1	1 error in overall parity bit	1 or 3 errors @

triple error detected[1]
a total of 3 errors in the previous frame @

Table 4.2 Increment to the OFD count for various decoder events.

increment to the OOF detection count	synd = 0	synd = 1
check-sum=0	reset count to 0	2#
check-sum=1	2#	1

triple errors detected
2

The transition probabilities associated with the increments 1 and 2 are denoted as p1 and p2, and the transition probability associated with resetting the OFD count back to 0 is denoted as p0. The transition probability associated with the increment for the triple errors event is denoted as p1u.

The triple error detection in a frame happens over 2 frame periods. First, an odd number of errors is detected at the end of a first frame period. The error correction unit (ECU) attempts to correct a single error; when the correction-location is not found at the end of the second frame period, the triple error detection signal is generated to indicate that at least 3 errors have occurred in the previous frame. Therefore, the increment to the OFD

---

[1] the error correction unit is only activated when an odd number of errors have been detected in the frame period - and the detection of triple error is obtained at the end of the decoding period.

@ Some combinations of triple errors in a frame yield syndromes which have correction locations pointing to positions outside the shortened code word. When this happens at least 3 errors must have occurred in the frame period.

# The probability p2 is obtained by adding the two probabilities associated with the increment value 2.

count for a triple error event happens after 2 frame periods (i.e. first an increment of 1 is made at the end of the first frame period and an additional increment of two is made at the end of the second frame period).

Before drawing the Markov chain state transition diagrams for the "successive-accummulation-to-c" schemes the model depicting the transitions from an arbitrary state N is first analyzed.

The possible transitions from an arbitrary state N are depicted in Fig. 4.1. These are the transitions to state 0, N+1, N+2, and N+3 with the corresponding transition probabilities p0, p1, p2, and p1u. (Note that 0, N, N+1, N+2, and N+3 are integer values denoting the actual value of the OFD count.) The transition to state N+3 requires 2 frame times with an intermediate transition to state N+1. In fact the transition to state N+3 never happens on its own because at the end of the second frame period a new increment (or transition) based on the number of errors detected in the second frame period immediately causes a transition to state NEW from state N+3. For this reason the time spent in state N+3 is infinitesimally small (or even identical to zero). A Markov model based on the type of transitions in Fig. 4.1 involves many complicated transitions and non-constant transition times between the branches and could be analyzed using very tedious procedures. The Markov model can be simplified if the state transitions in Fig. 4.1 are modified into the ones shown in Fig. 4.2.

There is no change made in the state transitions to states 0, N+1, and N+2. The transition to state N+3 is done in one step without the intermediate state and it is assumed that it takes only 1 frame time to complete. With this modification, the transition from state N+3 to state NEW also takes one frame time. The immediate impression is that the model in Fig. 4.2 is an approximate model of the exact model. However as long as state N+3 is not the absorbing (OOF) state c (or more precisely, N+3 < c), the transition time (duration) and probability involved in transferring from state N to NEW described by the two models are identical. Therefore the two models will give identical absorption times. In the case when the state N+3 is the absorbing state c or N+3 ≥ c and N+1 < c (because when N+1 ≥ c, the transition to state c only takes 1 frame period, hence the model in Fig. 4.2 applies), the model in Fig. 4.2 becomes inaccurate because the transition from state N to c (or N+3) actually takes 2 frame periods rather than 1. To circumvent this problem, the model in Fig. 4.3 is used.

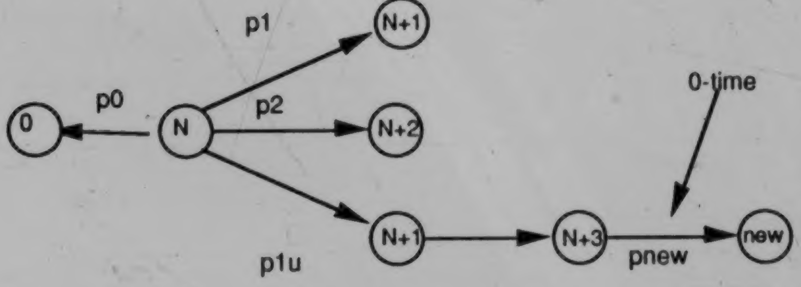

p1
N+1
0-time
p0
0
N
p2
N+2
N+1
N+3
new
p1u
pnew

Fig. 4.1 State transitions for state "N".

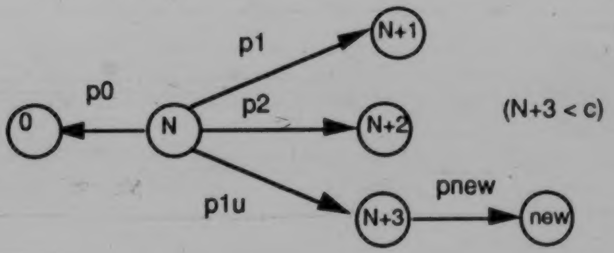

p1
N+1
p0
0
N
p2
N+2
(N+3 < c)
pnew
p1u
N+3
new

Fig. 4.2 Equivalent state transitions for state "N" (when N+3 < c).

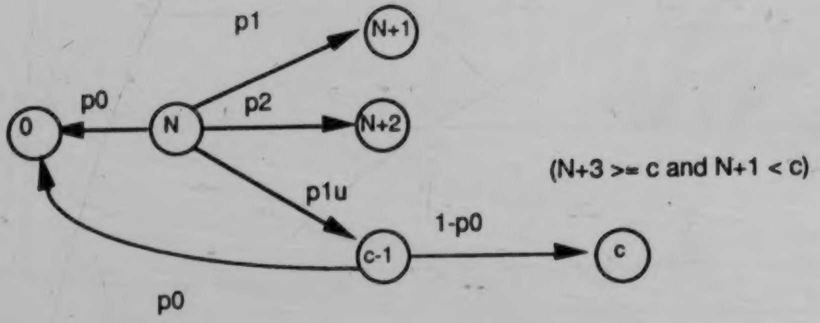

p1
N+1
p0
p2
0
N
N+2
(N+3 >= c and N+1 < c)
p1u
1-p0
c-1
c
p0

Fig. 4.3 Equivalent state transitions for state "N" (when N+3 ≥ c and N+1 < c).

The transition to the intermediate state c-1 rather than state N+1 is made because the former guaranties (except for the transition resetting to state 0) the transition to state c in the second frame period whereas the latter does not. Now the transition time and probability between states N and c are exact. Using the models in Fig. 4.2 and 4.3, the Markov chain state transition diagrams for the "successive-accummulation-to-c" scheme for values of c = 6, 7, and 8 are shown in Fig. 4.4 (a, b, and c).

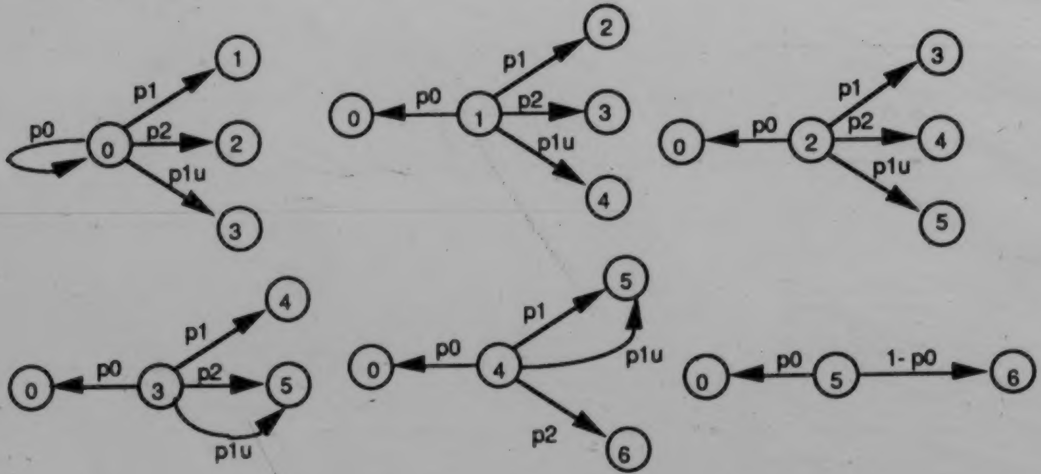

p0
0
p1
1
p2
2
p1u
3
0
p0
1
p1
2
p2
3
p1u
4
0
p0
2
p1
3
p2
4
p1u
5
0
p0
3
p1
4
p2
5
p1u
0
p0
4
p1
5
p1u
p2
6
0
p0
5
1- p0
6

Fig. 4.4a Markov model for the SC OFD scheme (c = 6).

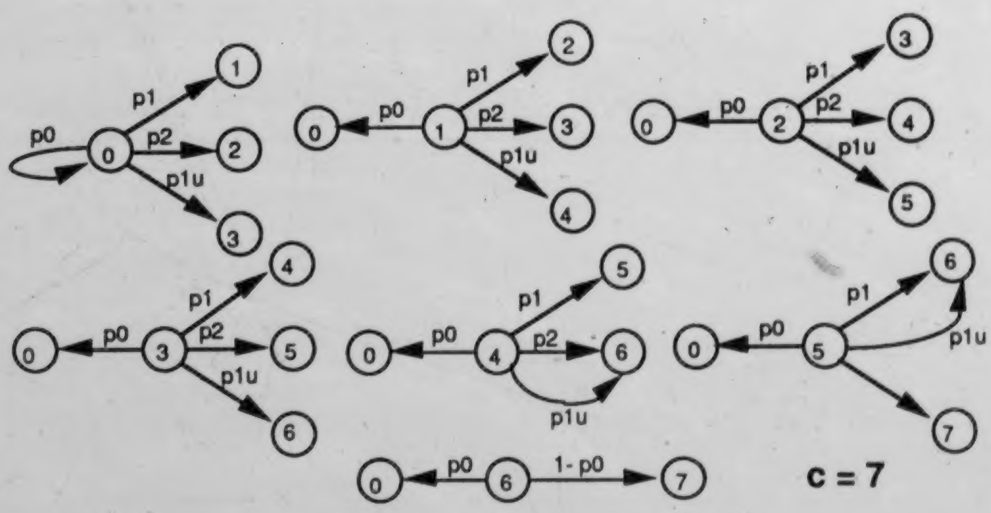

p0
p1
p2
p1u
1-p0
0
1
2
3
4
5
6
7
c = 7

Fig. 4.4b Markov model for the SC OFD scheme (c = 7).

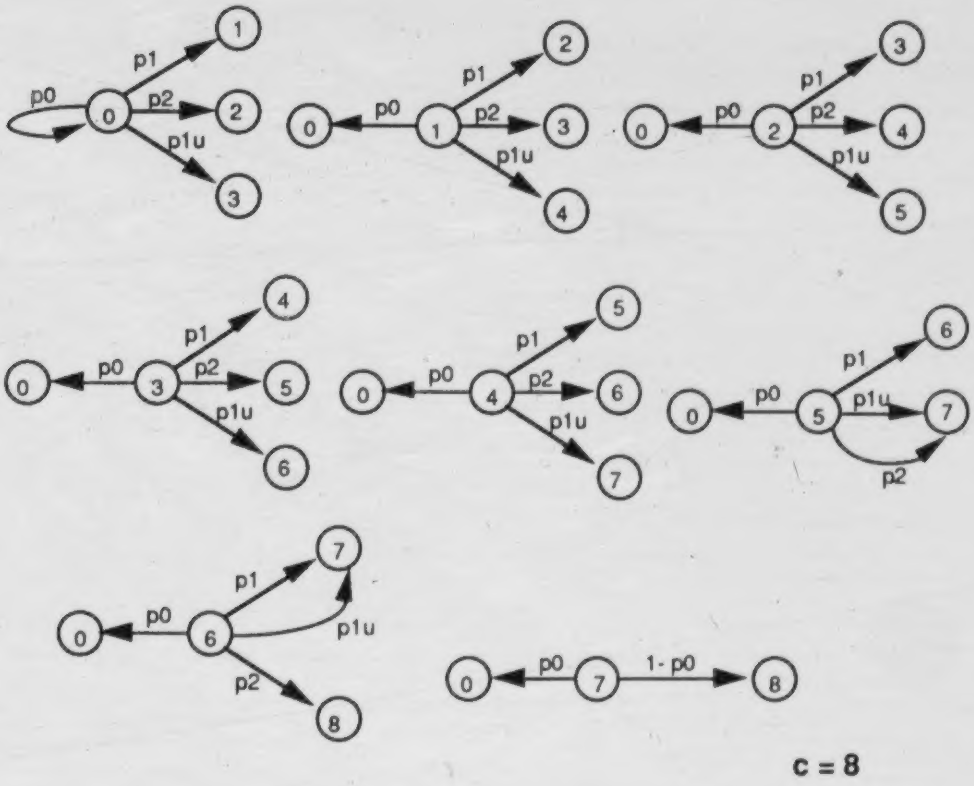

p0
p1
p2
p1u
0
1
2
3
4
5
6
7
8
1- p0
c = 8

Fig. 4.4c Markov model for the SC OFD scheme (c = 8).

The state transition matrices are derived from the Markov models and are shown below:

c = 6.

$$\begin{matrix} p0 & p1 & p2 & p1u & 0 & 0 & 0 \\ p0 & 0 & p1 & p2 & p1u & 0 & 0 \\ p0 & 0 & 0 & p1 & p2 & p1u & 0 \\ p0 & 0 & 0 & 0 & p1 & p2+p1u & 0 \\ p0 & 0 & 0 & 0 & 0 & p1+p1u & p2 \\ p0 & 0 & 0 & 0 & 0 & 0 & 1-p0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{matrix}$$

c = 7.

$$\begin{matrix} p0 & p1 & p2 & p1u & 0 & 0 & 0 & 0 \\ p0 & 0 & p1 & p2 & p1u & 0 & 0 & 0 \\ p0 & 0 & 0 & p1 & p2 & p1u & 0 & 0 \\ p0 & 0 & 0 & 0 & p1 & p2 & p1u & 0 \\ p0 & 0 & 0 & 0 & 0 & p1 & p2+p1u & 0 \\ p0 & 0 & 0 & 0 & 0 & 0 & p1+p1u & p2 \\ p0 & 0 & 0 & 0 & 0 & 0 & 0 & 1-p0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{matrix}$$

c = 8.

$$\begin{matrix} p0 & p1 & p2 & p1u & 0 & 0 & 0 & 0 & 0 \\ p0 & 0 & p1 & p2 & p1u & 0 & 0 & 0 & 0 \\ p0 & 0 & 0 & p1 & p2 & p1u & 0 & 0 & 0 \\ p0 & 0 & 0 & 0 & p1 & p2 & p1u & 0 & 0 \\ p0 & 0 & 0 & 0 & 0 & p1 & p2 & p1u & 0 \\ p0 & 0 & 0 & 0 & 0 & 0 & p1 & p2+p1u & 0 \\ p0 & 0 & 0 & 0 & 0 & 0 & 0 & p1+p1u & p2 \\ p0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1-p0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{matrix}$$

Fig.4.5 State transition probability matrices of the Shortened Code OFD schemes (for c=6, 7, & 8)

4.1.2 OOF Detection Times

To obtain the PGF for the OFD times the probabilities associated with various decoder events obtained as a result of misaligned frames are shown in Table 4.3.

Table 4.3 Probabilities associated with various decoder events.

Probability of the event	synd = 0	synd = 1
check-sum=0	$p_m p_s$	$s\, q_m q_s$
check-sum=1	$p_m q_s$	$q_m q_s$

triple errors detected
$u\, q_m q_s$

where $p_m = 2^{-11}$ is the probability of having a zero syndrome for a misaligned frame, and $q_m = 1 - p_m$. $p_s = 0.5$ is the probability of having an even overall check-sum for the misaligned frame. $q_s = 1 - p_s$. s denotes the probability of having a syndrome (of the misaligned frame) which can be used to successfully locate an erroneous position within the shortened code word. It is estimated as[1] :

length of the shortened code/ length of the parent code =1359/2047.

u = 1 - s is the probability of having a syndrome (of the misaligned frame) which cannot be used to successfully locate an erroneous position within the shortened code word.

The probabilities p0, p1, p2, and p1u are obtained from Table 4.3. Using their assigned values and solving the state transition matrices involved, the PGF's are obtained.

From the PGF's, the mean, standard deviation, and other percentile statistics are obtained (using the steps outlined in 2.4.1) as listed in Table 4.4. The corresponding statistics obtained experimentally are listed in Table 4.5. Once again the values are expressed in units of F-bit intervals.

Table 4.4 Theoretical OFD times for the SC OFD scheme.

c =	Mean	Standard Deviation	99.5 percentile	99.8 percentile	99.9 percentile
6	30.01	5.41	48	48	48
7	34.36	5.91	48	56	56
8	38.73	6.29	56	56	64

Table 4.5 Experimental OFD times for the SC OFD scheme.

c =	Mean	Standard Deviation	99.5 percentile	99.8 percentile	99.9 percentile
6	30.05	5.41	48	48	48
7	34.35	5.93	48	56	56
8	38.72	6.26	56	56	64

---

[1] The syndromes obtained during the OOF state are random patterns, therefore the correction locations they point to can be approximated as a random variable uniformly distributed over the span of the original parent code.

The probability distributions of the OFD times for c = 6, 7, and 8 are obtained by expanding the respective PGF's, and are shown in Fig. 4.6. The probability distributions obtained analytically and experimentally for c=7 are compared in Fig. 4.7. It is found that all the analytical results are consistent with the experimental ones.

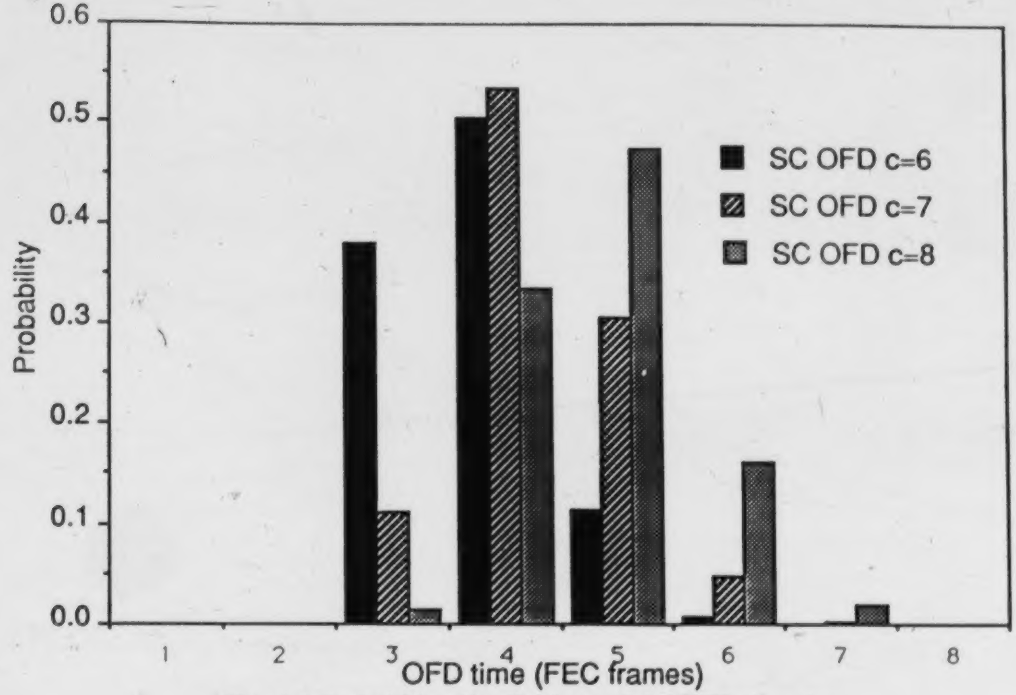


Fig. 4.6 Probability distributions of the OFD time for the SC OFD schemes (for c = 6, 7, and 8).

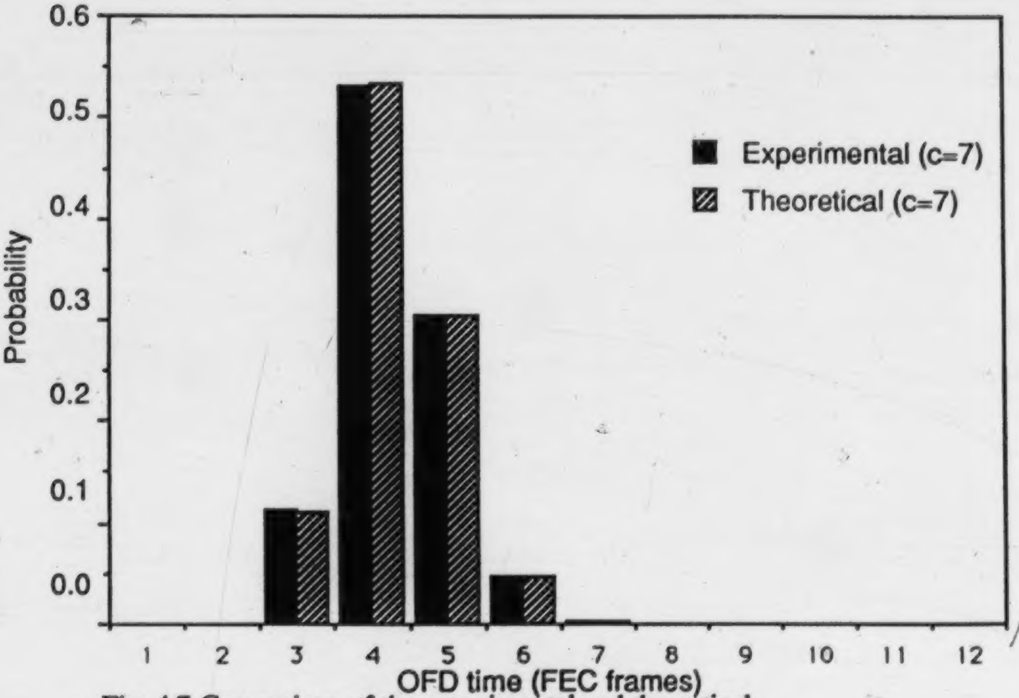


Fig. 4.7 Comparison of the experimental and theoretical probability distributions of the OFD time for the SC-OFD scheme (c=7).

4.1.3 Misframe Times

As for the PGF's for the misframe times, the probabilities associated with various decoder events (as a result of error occurrences in aligned frames) are derived from Table 4.1 and tabulated in Table 4.6.

Table 4.6 Probabilities associated with various decoder events (error-events).

Probability of the event	synd = 0	synd = 1
check-sum=0	q_e^{1360} $+ A\ p_e^4 q_e^{1360}$	$1360C_2\, p_e^2 q_e^{1358}$ $+ B\ 1360C_4\, p_e^4 q_e^{1356}$
check-sum=1	$p_e q_e^{1359}$	$s[1360C_3\, p_e^3 q_e^{1357}]$

triple errors detected
$u[1360C_3\, p_e^3 q_e^{1357}]$

where $p_e = BER_{channel}$, and $q_e = 1 - p_e$. nC_k is the number of combination for choosing k out of n items. A is the conditional probability of having a zero syndrome when there are 4 errors in the frame, it is estimated as:

$$A = \frac{\text{the number of combinations of 4 errors in a code word that produce a valid code word}}{\text{the possible total number of combinations of 4 errors in a code word}} = \frac{W_4}{nC_4}$$

where W_4 is also equal to the total number of valid code words that have a weight of 4, it is derived in Appendix B. B = 1 - A.

When estimating the misframe times using probability generating functions, meaningful results are only obtained if the PGF ($P_X(x)$) satisfies the following criterion,

$$P_X(1) = 1 \tag{4.1}$$

Equation (4.1) is only satisfied if the sum of all the transition probabilities involved is equal to 1, we shall called this the sum-to-one criterion. However, the sum of the probabilities obtained from the combined values of the event-probabilities in Table 4.6 cannot be equal to 1, because each of the event-probabilities in the table only consists of the probabilities of having up to 4 errors. The sum-to-one criterion can only be achieved if each event-probabilities in Table 4.6 includes the probabilities of having 0 to 1360 errors. In practice, this is impossible. Therefore, to satisfy the sum-to-one criterion when estimating the misframe times, the following steps are performed when obtaining the transition probabilities.

i. each of the event-probabilities is approximated as shown in Table 4.6.

ii. the transition probabilities p0, p1, p1u, p2u, p2 are assigned with the appropriate values in Table 4.6.

iii. the transition probability p2 is reassigned as: p2 = 1 - (p0+p1+p1u+p2u).

iv. using the assigned values for the transition probabilities and solving the PGF's involved, the misframe times are obtained.

v. to verified the accuracy of the estimated misframe times, a second estimate is obtained by repeating steps ii. and reassigning p0 = 1 - (p1+p2+p1u+p2u).

vi. the misframe times estimated in steps iv. and v. are almost identical.

The estimated average MF times, T_{MF}'s (or their logarithms), in units of F-bit intervals, with BER ranging from 10^{-4} to 10^{-10} for c = 6, 7, and 8 are tabulated in Table 4.7. The T_{MF}'s are also plotted in Fig. 4.8.

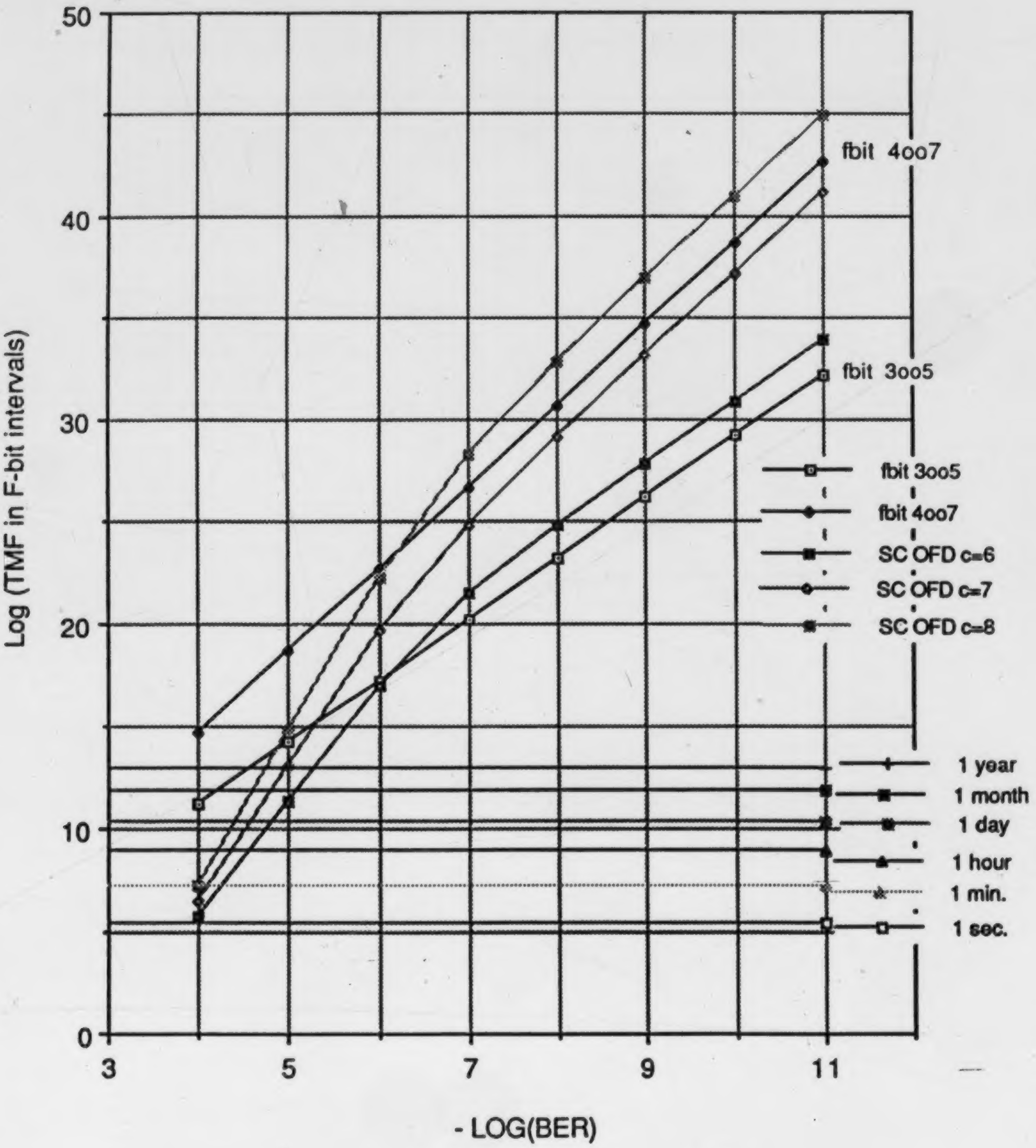


Fig. 4.8 Comparison of the TMF's for F-bit and SC OFD schemes.

Table 4.7 MF times of the SC OFD scheme.

Log(BER)	-4	-5	-6	-7	-8	-9	-10
Log(T_{MF}) (c=6)	5.6 (1.5 secs)	11.3 (8.8 days)	16.9	21.4	24.84	27.90	30.90
Log(T_{MF}) (c=7)	6.38 (9.1 secs)	13.02 (1.26 yrs)	19.57	24.88	29.14	33.16	37.17
Log(T_{MF}) (c=8)	7.134 (48 secs)	14.73 (65 yrs)	22.21	28.24	32.81	36.89	40.90

It is evident that the T_{MF}'s at the degraded BER level $=10^{-5}$ are not large enough when c = 6 is used. When c = 7 is used, the corresponding $T_{MF} = 10^{13}$ (F-bit intervals) or 1.2 years is sufficiently long. Therefore c = 7 is chosen as the OOF detection confirmation for the SC OOF detection scheme. The misframe times of this scheme are compared with other schemes in Chapter 5.

4.2 The Hybrid OOF Detection Scheme

This scheme uses the syndromes, overall check-sums, triple error detection signals, and the masterframe overhead bits (M, P, and X) to accelerate the OOF detection in FEC framing.

The master frame structure of the DS3 signal is shown in Fig. 4.9; each FEC frame contains two DS3 frames and hence two masterframe overhead bits. From here on the masterframe overhead bits will be collectively denoted as the MPX bits.

The MPX bits follow a periodic 0-1-0-P-P-X-X pattern, where P is equal to the overall check-sum of the previous master frame and X is reserved for customer use and is random. Both P and X bits are duplicated.

M_0 [679]	M_1 [679]	M_0 [679]	P [679]	P [679]	X [679]	X [679]

Fig. 4.9 The DS3 master frame structure.

[679] are the remaining bits in each DS3 frame.

4.2.1 State Transitions in the Markov Model

As before the "successive-accummulation-to-c" criterion is used where the increment to the OFD count is equal the most probable number of errors that can be detected by the error detection circuit. Here an increment of 1 to the OFD count is made when a single error has been detected (not a specific bit) in a frame. An increment of 2 to the OFD count is made when an error has been detected in a specific bit (such as the overall parity bit, M, P, or X bit) or when two errors have been detected in a frame. Similarly an increment of 3 (or 4) to the OOF detection count is added when three (or four) errors have been detected in a frame. Finally, an additional increment of 2 to the OOF detection count is added when there is triple error detection at the end of the frame period (only 2 is added because an increment of 1 has been added at the end of the previous frame period). Sometimes, errors can be detected in both the MPX bits and the bits in the rest of the frame.

Using the rules for associating the decoder events with the number of errors in a frame described in Subsec. 4.1.1, and also taking into account that the 2 examined MPX bits are part of the FEC frame, the most probable and the next most probable number of additional errors in the rest of the frame (excluding the MPX bit errors) associated with various decoder events are determined as shown in Table 4.8.

Table 4.8 Number of errors associated with various decoder events and number of MPX violations

number of errors in frame	synd = 0 check-sum=0 @	synd = 0 check-sum=1 #	synd = 1 check-sum=1	synd = 1 check-sum=0	triple error detected *
0 MPX bit error	0 or 4 total = 0 or 4	error in overall parity bit total = 1	1 or 3 * total = 1 or 3	2 or 4 total = 2 or 4	+2 in the previous frame
1 MPX bit error	+3 total =4	+2 total =3	+0 or +2* total =1 or 3	+1 and +3 total=2 or 4	+2 in the previous frame
2 MPX bit errors	+2 total =4	+1 total =3	+1 total =3	+0 and +2 total =2 or 4	

Note: +m indicates m errors are detected in the rest of the frame in addition to the number of MPX bit errors specified in column one.

The increments to the OFD count corresponding to various combinations of decoder events and the number of MPX bits violation are shown in Table 4.9.

Table 4.9 Increment values associated with various combinations of decoder events

increment to the OOF detection count	synd = 0 check-sum=0	synd = 0 check-sum=1	synd = 1 check-sum=1	synd = 1 check-sum=0	triple errors detected
0 MPX bit violation	reset back to 0	2	1	2	2
1 MPX bit violation	5	4	2	3	2
2 MPX bit violations	6	5	5	4	

Note an increment of 2 is associated with each detected MPX error.

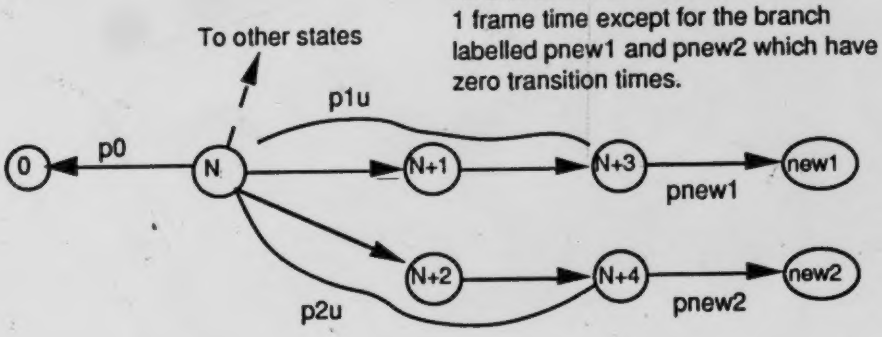
@Zero syndromes and even overall check-sums are obtained for frames with certain combinations of quadruple errors.

# Zero syndromes and odd overall check-sums are obtained for frames with certain combinations of triple errors.

* Some combinations of triple errors in a frame yield syndromes which have correction locations pointing to positions outside the shortened code word. When this happens at least 3 errors must have occurred in the frame period, but the increment of 2 rather than 3 is added when this event is detected because an increment of 1 has been added in the previous frame period.

The symbols p1, p2, p3, p4, p5, and p6 denote the probabilities of having the corresponding increments of 1 to 6. The symbol p1u denotes the probability of having a triple error detection (at the end of a frame period) when a non-zero syndrome and an odd overall check-sum together with no MPX bit error have been detected in the previous frame period. The symbol p2u denotes the probability of having a triple error detection (at the end of a frame period) when a non-zero syndrome and an odd overall check-sum together with a single MPX bit error have been detected in the previous frame period. Once again the transition times associated with the triple error detections (the probabilities p1u and p2u) are 2 frame periods.

The part of the models in Fig 4.2 and 4.3 modelling the transitions due to a triple error detection can be applied to this scheme with the following modifications. Since there are two possible transitions due to triple error detections the model in Fig. 4.1 is converted into the model in Fig. 4.10.



All branches have a transition time = 1 frame time except for the branch labelled pnew1 and pnew2 which have zero transition times.

Fig. 4.10 State transitions for state "N".

The model in Fig. 4.10 is converted into the models in Fig. 4.11 when N+4 < c.

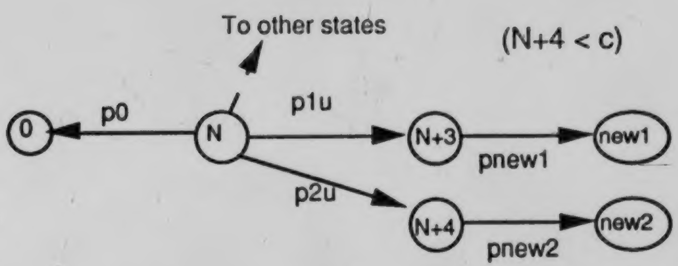

To other states
(N+4 < c)
0
p0
N
p1u
N+3
pnew1
new1
p2u
N+4
pnew2
new2

Fig. 4.11 Equivalent state transitions for state "N" (when N+4 < c).

The model in Fig. 4.12 applies when $N+3 \geq c$ and $N+1 < c$. The model in Fig. 4.13 applies when $N+4 \geq c$ and $N+2 < c$.

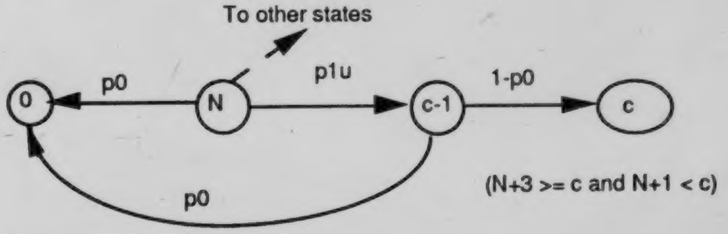

To other states
0
p0
N
p1u
c-1
1-p0
c
p0
(N+3 >= c and N+1 < c)

Fig. 4.12 Equivalent state transitions for state "N" (when N+3 ≥ c and N+1 < c).

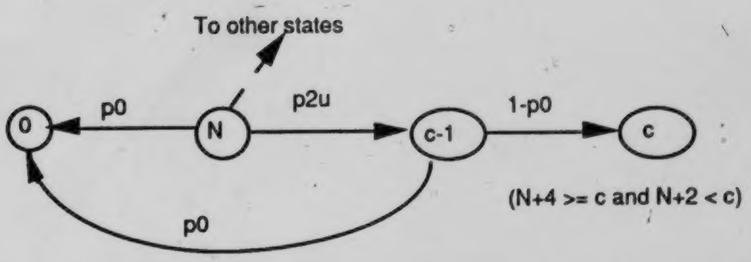

To other states
0
p0
N
p2u
c-1
1-p0
c
p0
(N+4 >= c and N+2 < c)

Fig. 4.13 Equivalent state transitions for state "N" (when N+4 ≥ c and N+2 < c).

The Markov chain state transition diagrams of the "successive-accummulation-to-c" schemes for values of c = 6, 7, and 8 are shown in Fig. 4.14 (a,b, and c).

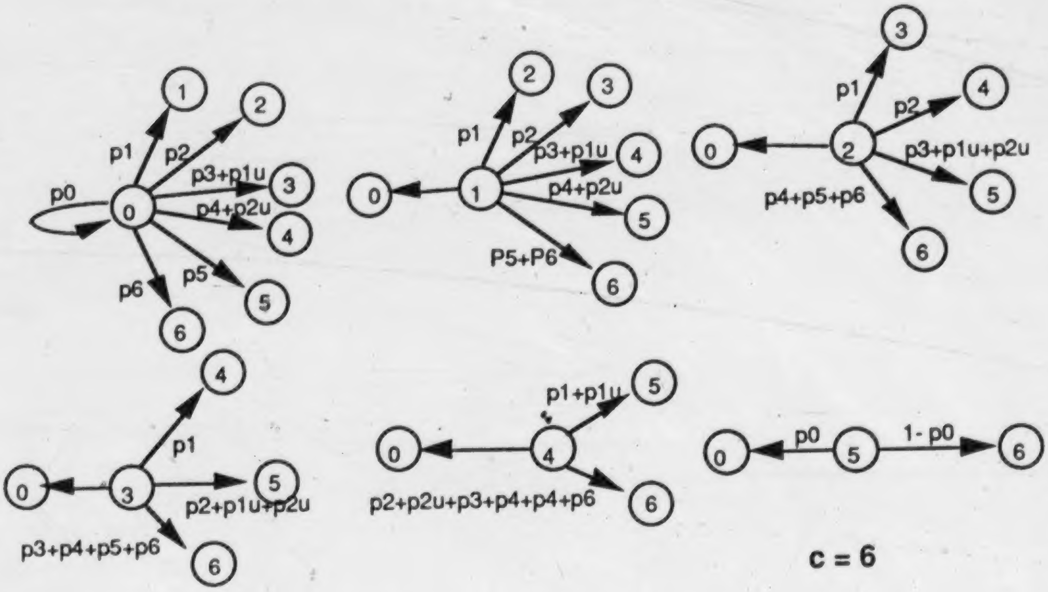

p0
p1
p2
p3+p1u
p4+p2u
p5
p6
p1
p2
p3+p1u
p4+p2u
P5+P6
p1
p2
p3+p1u+p2u
p4+p5+p6
p1
p2+p1u+p2u
p3+p4+p5+p6
p1+p1u
p2+p2u+p3+p4+p4+p6
p0
1- p0
0
1
2
3
4
5
6
c = 6

Fig. 4.14a Markov model for the Hybrid OFD scheme (c = 6).

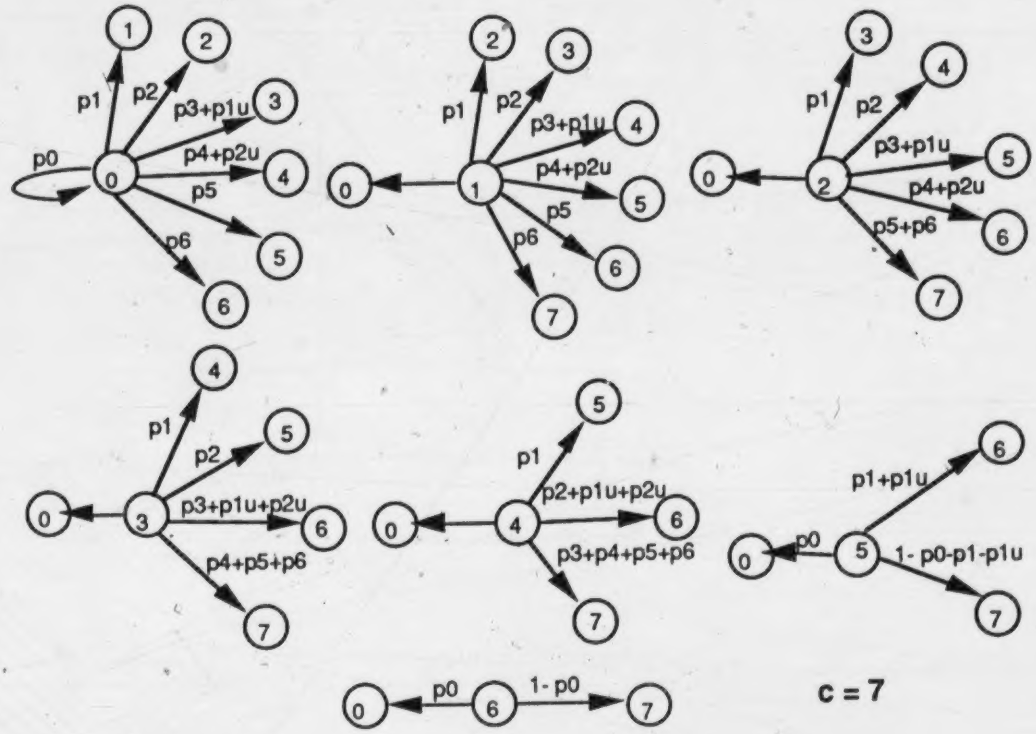

p0
p1
p2
p3+p1u
p4+p2u
p5
p6
p1
p2
p3+p1u
p4+p2u
p5
p6
p1
p2
p3+p1u
p4+p2u
p5+p6
p1
p2
p3+p1u+p2u
p4+p5+p6
p1
p2+p1u+p2u
p3+p4+p5+p6
p1+p1u
p0
1- p0-p1-p1u
p0
1- p0
0
1
2
3
4
5
6
7
c = 7

Fig. 4.14b Markov model for the Hybrid OFD scheme (c = 7).

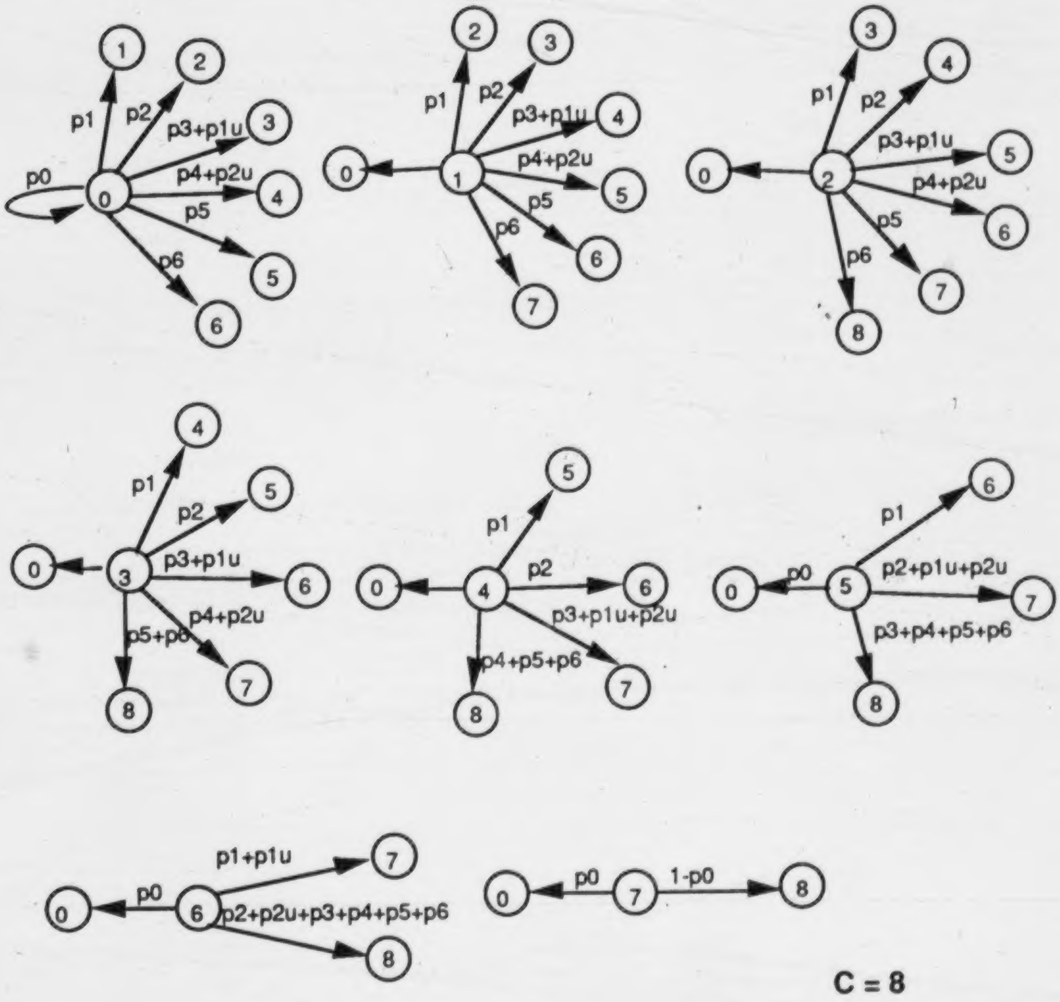

1
2
3
4
5
6
p0
p1
p2
p3+p1u
p4+p2u
p5
p6
0
0
1
2
3
4
5
6
7
p1
p2
p3+p1u
p4+p2u
p5
p6
0
2
3
4
5
6
7
8
p1
p2
p3+p1u
p4+p2u
p5
p6
0
3
4
5
6
7
8
p1
p2
p3+p1u
p4+p2u
p5+p6
0
4
5
6
7
8
p1
p2
p3+p1u+p2u
p4+p5+p6
0
5
6
7
8
p0
p1
p2+p1u+p2u
p3+p4+p5+p6
0
6
7
8
p0
p1+p1u
p2+p2u+p3+p4+p5+p6
0
7
8
p0
1-p0
C = 8

Fig. 4.14c Markov model for the Hybrid OFD scheme (c = 8).

The state transition probability matrices are derived for the models and are shown in Fig. 4.15. The PGF of the OFD and MF times can be obtained (from the matrices) by assigning the appropriate values to the transition probabilities.

$c = 6$

$$\begin{array}{lllllll}
p0 & p1 & p2 & p3+p1u & p4+p2u & p5 & p6 \\
p0 & 0 & p1 & p2 & p3+p1u & p4+p2u & p5+p6 \\
p0 & 0 & 0 & p1 & p2 & p3+p1u+p2u & p4+p5+p6 \\
p0 & 0 & 0 & 0 & p1 & p2+p1u+p2u & p3+p4+p5+p6 \\
p0 & 0 & 0 & 0 & 0 & p1+p1u & p2+p2u+p3+p4+p5+p6 \\
p0 & 0 & 0 & 0 & 0 & 0 & 1-p0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0
\end{array}$$

$c = 7$

$$\begin{array}{llllllll}
p0 & p1 & p2 & p3+p1u & p4+p2u & p5 & p6 & 0 \\
p0 & 0 & p1 & p2 & p3+p1u & p4+p2u & p5 & p6 \\
p0 & 0 & 0 & p1 & p2 & p3+p1u & p4+p2u & p5+p6 \\
p0 & 0 & 0 & 0 & p1 & p2 & p3+p1u+p2u & p4+p5+p6 \\
p0 & 0 & 0 & 0 & 0 & p1 & p2+p1u+p2u & p3+p4+p5+p6 \\
p0 & 0 & 0 & 0 & 0 & 0 & p1+p1u & p2+p2u+p3+p4+p5+p6 \\
p0 & 0 & 0 & 0 & 0 & 0 & 0 & 1-p0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0
\end{array}$$

$c = 8$

$$\begin{array}{lllllllll}
p0 & p1 & p2 & p3+p1u & p4+p2u & p5 & p6 & 0 & 0 \\
p0 & 0 & p1 & p2 & p3+p1u & p4+p2u & p5 & p6 & 0 \\
p0 & 0 & 0 & p1 & p2 & p3+p1u & p4+p2u & p5 & p6 \\
p0 & 0 & 0 & 0 & p1 & p2 & p3+p1u & p2u+p4 & p5+p6 \\
p0 & 0 & 0 & 0 & 0 & p1 & p2 & p1u+p2u+p3 & p4+p5+p6 \\
p0 & 0 & 0 & 0 & 0 & 0 & p1 & p1u+p2+p2u & p3+p4+p5+p6 \\
p0 & 0 & 0 & 0 & 0 & 0 & 0 & p1+p1u & 1 - p0 - p1 - p1u \\
p0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1-p0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0
\end{array}$$

Fig. 4.15 State transition probability matrices for the Hybrid OFD scheme.

4.2.2 Out-of-frame Detection Times

To obtain the PGF for the OFD times, the probabilities associated with various decoder events and the number of MPX bit violations are listed in Table 4.10. (Here the decoded syndromes, overall check-sums, the detected number of MPX bit violations are obtained from mis-aligned frames and bit positions).

Table 4.10 Probabilities associated with various decoder events and number of MPX violations.

Probability of the event.	synd = 0 check-sum=0	synd = 0 check-sum=1	synd = 1 check-sum=1	synd = 1 check-sum=0	triple errors detected
0 MPX bit violations	$p_m\, p_s\, p0v$	$p_m\, q_s\, p0v$	$q_m\, q_s\, p0v\, s$	$q_m\, p_s\, p0v$	$q_m\, q_s\, p0v\, u$
1 MPX bit violations	$p_m\, p_s\, p1v$	$p_m\, q_s\, p1v$	$q_m\, q_s\, p1v\, s$	$q_m\, p_s\, p1v$	$q_m\, q_s\, p1v\, u$
2 MPX bit violations	$p_m\, p_s\, p2v$	$p_m\, q_s\, p2v$	$q_m\, q_s\, p2v$	$q_m\, p_s\, p2v$	

where p_m, q_m, p_s, q_s, s, and u are the same as those specified in Subsec. 4.1.2. p0v, p1v,and p2v are the probabilities of having 0, 1, and 2 out of the two examined bits(the 2 bits obtained from the misaligned MPX bit positions locked onto by the framing circuit) violating the MPX bit pattern in the decoded frame.

The values of p0v, p1v, and p2v should respectively be equal to 1/4, 1/2, and 1/4 if the MPX bit pattern is fixed. However, because the duplicated X-bits are reserved for customers' applications and are random, for OOF detection purposes only the second of the duplicated X-bits of each masterframe can be used by the OOF detection circuit to check whether it duplicates the first X-bit (the first examined X-bit appears to the detection circuit as if it never violates the MPX bit pattern). To obtain the probabilities p0v, p1v, and p2v, the numbers of MPX bits that the OOF detection circuit can use for a series of 7 FEC frames (7 is examined here because the pattern of the MPX bits repeats itself every 7 frames) are shown in Fig. 4.16.

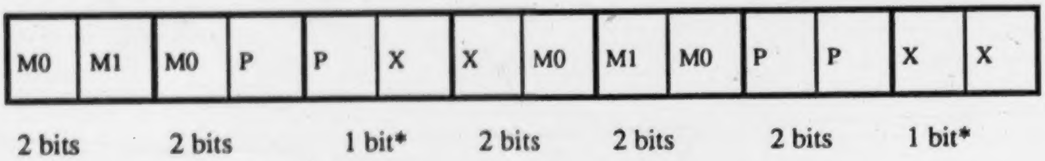


Fig. 4.16 The number of MPX bits that can use for OOF detection purposes for 7 FEC frames.

*Note: the first X bit appears to the detection circuit as if it always conforms to the MPX pattern.

From Fig. 4.16, we have:

The probability of having both of the two examined bits simulating the MPX bit pattern is:

$$p0v = 1/7[1/4 + 1/4 + 1/2 + 1/4 + 1/4 + 1/4 + 1/2] = 9/28$$

The probability of having only one of the two examined bits simulating the MPX bit pattern is:

$$p1v = 1/7[1/2 + 1/2 + 1/2 + 1/2 + 1/2 + 1/2 + 1/2] = 1/2$$

And the probability of having both of the two examined bits violating the MPX bit pattern is:

$$p2v = 1/7[1/4 + 1/4 + 0 + 1/4 + 1/4 + 1/4 + 0] = 5/28$$

The transition probabilities p1, p2, ... ,and p6 are obtained by combining tables 4.9 and 4.10 (p1u and p2u are obtained from the last column these tables). The PGF's are obtained by using the assigned values of the probabilities and solving the state transition probability matrices.

From the PGF's, the mean OFD times, their standard deviations and other percentile statistics are derived and shown in Table 4.11. The corresponding experimental values are shown in Table 4.12. The probability distributions of the OF times, obtained by expanding the respective PGF's, for c = 6, 7, and 8 are shown in Fig. 4.17. The probability distribution of the OFD times for c = 7 obtained using computer simulations are compared with those obtained analytically in Fig. 4.18; it is found that there is negligible difference between the two probability distributions.

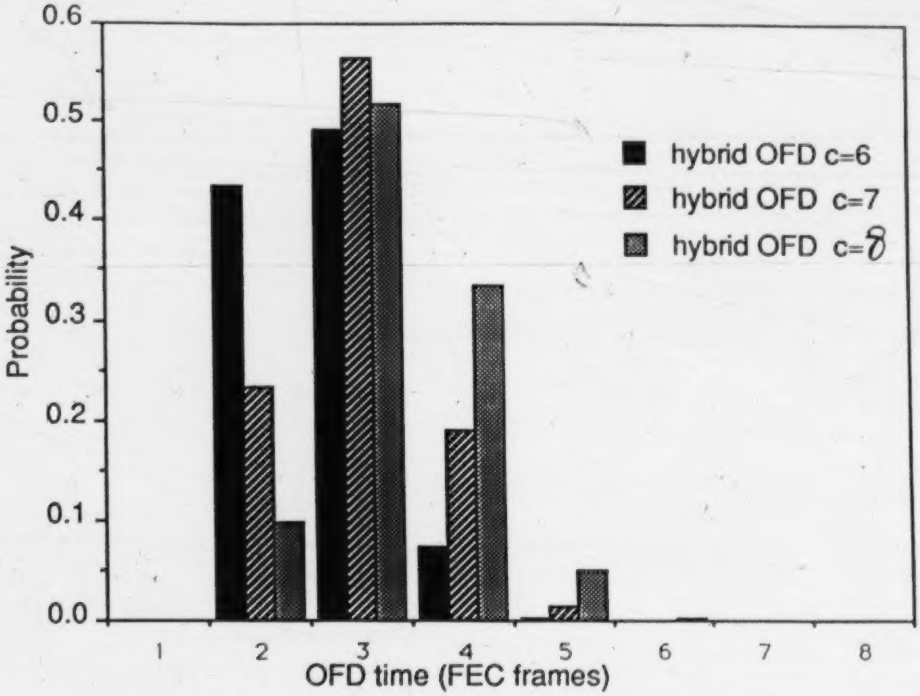


Fig. 4.17 Probability distributions of the OFD time for the Hybrid OFD scheme (for c= 6, 7, 8).

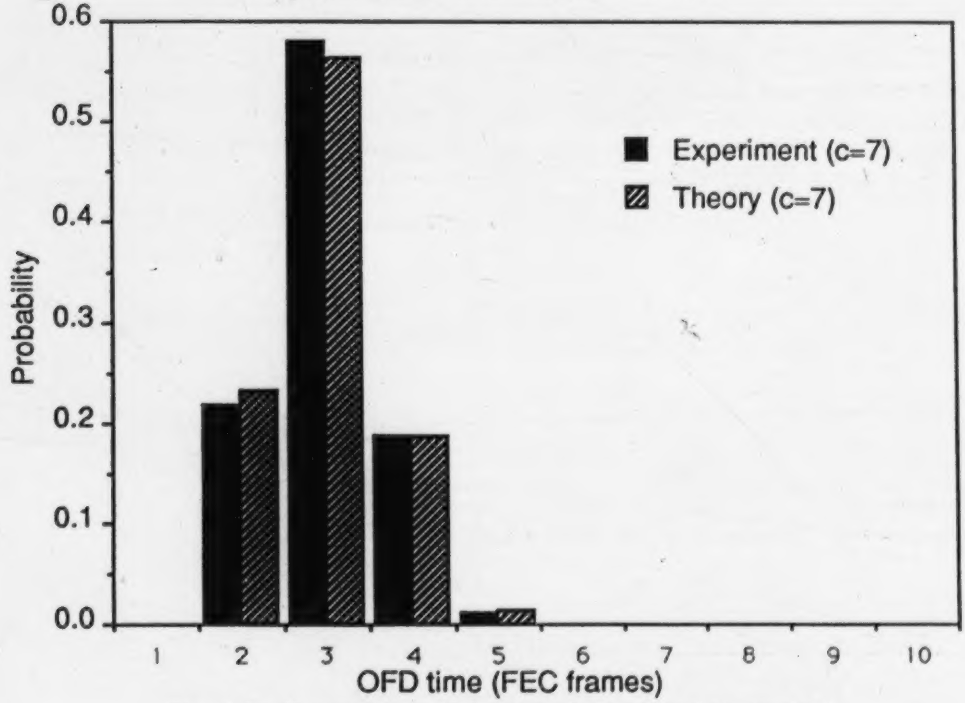


Fig. 4.18 Comparison of the experimental and theoretical probability distributions of OFD time for the Hybrid OFD scheme (c=7) .

Table 4.11 Theoretical OFD times for the Hybrid OFD scheme.[1]

c =	Mean	Standard Deviation	99.5 percentile	99.8 percentile	99.9 percentile
6	21.17	5.02	32	40	40
7	23.89	5.56	40	40	40
8	26.76	5.85	40	48	48

Table 4.12 Experimental OFD times for the Hybrid OFD scheme.[1]

c =	Mean	Standard Deviation	99.5 percentile	99.8 percentile	99.9 percentile
6	21.16	4.95	32	40	40
7	23.95	5.43	40	40	40
8	26.78	5.70	40	48	48

4.2.3 Misframe Times

To obtain the PGF's of the MF times, the probabilities associated with various combination of decoder events and the number of MPX bit errors (obtained as a result of actual errors in aligned frames) are derived from Table 4.8 and listed in Table 4.13. Each of the transition probabilities is assigned the value corresponding to the combination of the detected number of errors associated with this transition.

Table 4.13 Probabilities associated with various decoder events

Probability of the event.	synd = 0 check-sum=0	synd = 0 check-sum=1	synd = 1 check-sum=1	synd = 1 check-sum=0	triple errors detected
0 MPX bit error	$qe^{1360} + A\ (n-2)C_4\ pe^4 qe^{1356}$	$pe\ qe^{1359}$	$(n-2)\ pe\ qe^{1359} + s\ (n-2)C_3\ pe^3\ qe^{1357}$	$(n-2)C_2\ pe^2\ qe^{1358} + B\ (n-2)C_4\ pe^4 qe^{1356}$	$u\ (n-2)C_3\ pe^3\ qe^{1357}$
1 MPX bit error	$A\ (n-2)C_3\ 2\ pe^4\ qe^{1356}$	$A\ (n-2)C_2\ 2\ pe^3\ qe^{1357}$	$2\ pe\ qe^{1359} + 2\ s\ (n-2)C_2\ pe^3\ qe^{1357}$	$(n-2)\ 2\ pe^2\ qe^{1358} + B\ 2\ (n-2)C_3\ pe^4\ qe^{1356}$	$u\ (n-2)C_2\ 2\ pe^3\ qe^{1357}$
2 MPX bit errors	$A\ (n-2)C_2\ pe^4\ qe^{1356}$	$A\ (n-2)\ pe3\ qe^{1357}$	$B\ (n-2)\ pe^3 qe^{1357}$	$pe^2\ qe^{1358} + B\ (n-2)C_2\ pe^4\ qe^{1356}$	

---

[1] All values are expressed in F-bit intervals.

When constructing Table 4.13 the MPX bit pattern is assumed to be fixed, that is the duplicated X-bits always have zero values. This assumption is made because it is much more difficult to estimate the misframe times involving random X-bits and the result might be inaccurate. This assumption will effectively make the estimated misframe values smaller than the actual misframe times when the X-bits are random. This is because having a fixed X-bits pattern means that more opportunities are available for the detection errors in the X-bit, and the misframe times obtained with this assumption are this lower bound values of the actual misframe times. In practice the lower bound values of the misframe times are sufficient for comparison purposes in our study.

For a fixed X-bit pattern the probabilities of having 0, 1, and 2 bit errors in the 2 examined MPX bits of each FEC frame are p_e^2, $2\, p_e\, q_e$, and q_e^2, with $p_e = BER_{channel}$ and $q_e = 1 - p_e$. The probability of having k errors in the frame of n=1360 bits is given by $nC_k\, p_e^k\, q_e^{n-k}$, and the probability of having k errors in the rest of the frame (excluding the 2 MPX bits) is $(n-2)C_k\, p_e^k\, q_e^{\,n-2-k}$. The probabilities A, B, s, and u are the same as those specified in Subsec. 4.1.2.

Each of the state transition probabilities is assigned with the appropriate combination of values in Table 4.13. Once again to satisfy equation (4.1), the steps outlined in Subsec. 4.1.3 are followed. p3 is reassigned as (1 - (p0+p1+p2+p4+p5+p6+p1u+p2u)). Using the assigned values for the transition probabilities the PGF's involved are solved and the mean MF times are obtained.

The estimated average MF times, T_{MF}'s (or their logarithms), expressed in units of F-bit intervals with BER values ranging from 10^{-4} to 10^{-10} for c = 6, 7, 8 are tabulated in Table 4.14 and are plotted in Fig. 4.19.

Table 4.14 MF times of the Hybrid OFD scheme.

Log(BER)	-4	-5	-6	-7	-8	-9	-10
Log(T_{MF}) (c=6)	5.7 (1.9 secs)	11 (4.4 days)	16	20	23	26	29
Log(T_{MF}) (c=7)	6.4 (9.5 secs)	13 (1.2 yrs)	19	23	27	31	35
Log(T_{MF}) (c=8)	7.2 (1 min)	15 (120 yrs)	21	27	31	35	39

It is evident that the T_{MF}'s at the degraded BER level of 10^{-5} are not large enough when c = 6 is used. When c = 7 is used the corresponding $T_{MF} = 10^{13}$ (F-bit intervals) or 1.2 years; which is sufficient. Therefore c = 7 is chosen as the OFD confirmation threshold for the Hybrid OOF detection scheme. The misframe times of the scheme are compared with other schemes in Chapter 5.

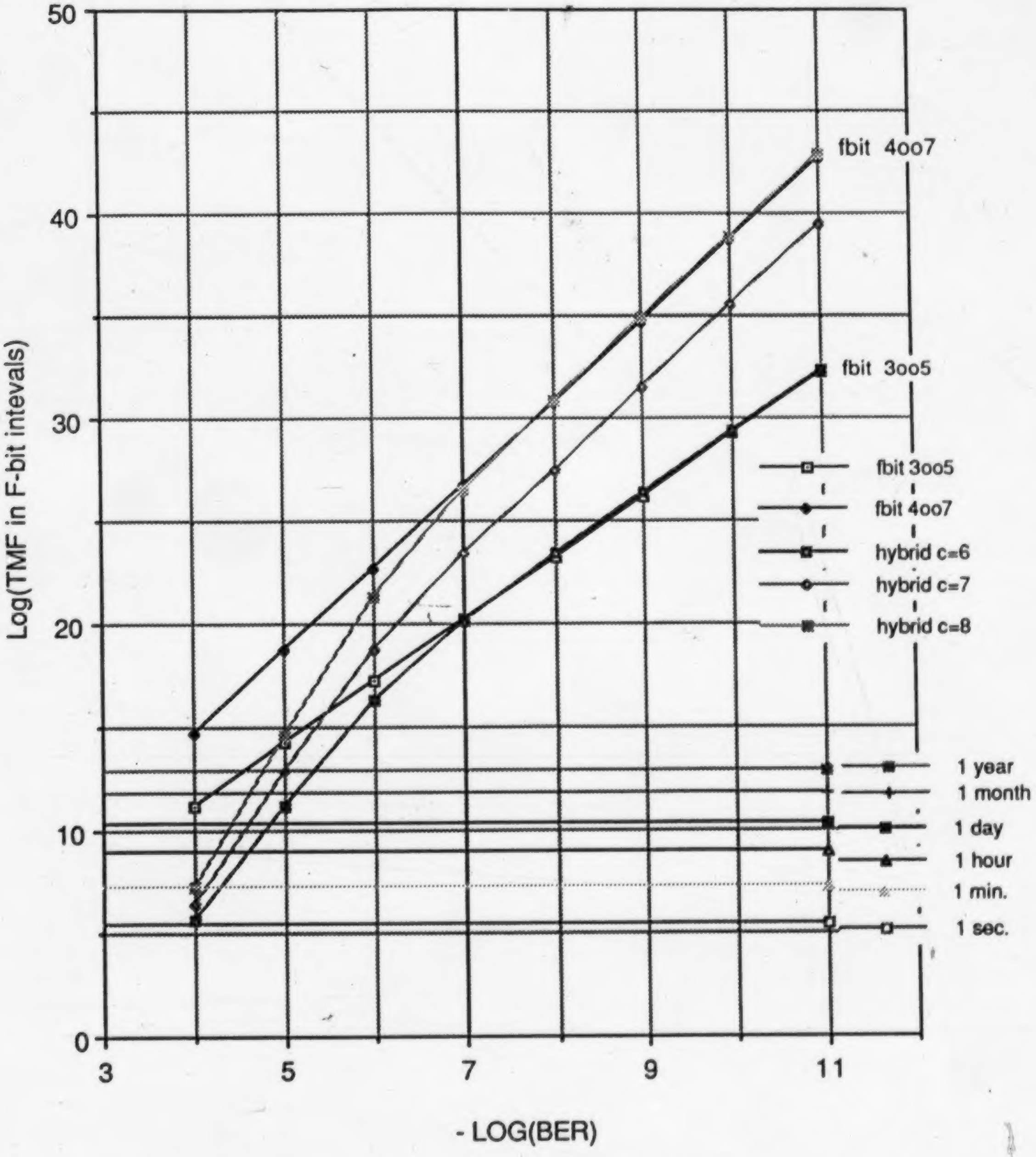


Fig. 4.19 Comparison of the TMF's for F-bit and Hybrid OFD schemes.

5. COMPARISON OF FEC AND F-BIT FRAMING

The OFD times of the F-bit (3-o-o-5) OFD, FEC OFD, SC OFD, and the Hybrid OFD schemes are compared in Table 5.1. (Note that only the OFD times for the selected confirmation threshold c in each scheme are compared.) The values are compared in units of F-bit interval.

Table 5.1. Comparison of the OFD times of F-bit and FEC framing.

	Mean	Standard Deviation	99.5 percentile	99.8 percentile	99.9 percentile
F-bit (3-o-o-5)	7.27	4.66	28	32	35
Basic FEC (c=6)	48.04	1.19	48	48	64
SC (c=7)	34.36	5.91	48	56	56
Hybrid (c=7)	23.89	5.56	40	40	40

The comparison in Table 5.1 shows that the OFD times of the FEC OFD scheme is worse than those of F-bit framing (specifically, its T_{OF} is 7 times longer than that of F-bit framing). However the T_{OF}'s of the SC OFD and Hybrid OFD schemes are only 4.7 times and 3.3 times, respectively, longer than that of F-bit framing. The 99.5 to 99.9 percentile values of the SC OFD scheme are not much larger than those of F-bit framing. The corresponding percentile values of the Hybrid OFD scheme are very close to those of F-bit framing. Specifically, the 99.9 percentile value is only 14% larger than that of F-bit framing. The introduction of the Hybrid OFD scheme has improved the T_{OF} time of FEC framing by a factor of 2.

The MRF, OFD, and the combined MRF and OFD times (in units of F-bit intervals) for the F-bit and FEC framing are compared in Table 5.2. (Note that the OFD times of the Hybrid OFD scheme are used in the comparison.)

Table 5.2 Comparison of F-bit and FEC framing in units of F-bit intervals.

	T_{RF}	99.9 percentile MRF	T_{OF}	99.9 percentile OFD	$T_{RF}+T_{OF}$	99.9 percentile MRF+OFD
F-bit	359	420	7.27 (3-o-o-5)	35	366.27	455
FEC	26.7	56	23.8 (Hybrid c=7)	40	50.5	96

Note: T_{RF} and T_{OF} are means of the RF and OF times respectively.

As shown in Table 5.2, the maximum average reframe time with FEC framing is 13 times less than with conventional F-bit framing. Although the T_{OF} of FEC framing (using the Hybrid OFD scheme) is almost 3.3 times as long as that of F-bit framing, its 99.9 percentile value is only marginally larger than that of F-bit framing. Because an OOF detection is always followed by a reframe, therefore it is logical to consider their combined value. The combined value of T_{OF} (using the Hybrid OFD) and T_{RF} for FEC framing (i.e. the duration of time between a loss of alignment and subsequent re-alignment), is one seventh of that for F-bit framing. The combined 99.9 percentile value is roughly one fifth of that for F-bit framing. The values in Table 5.2 are converted to actual times and compared in Table 5.3.

Table 5.3. Comparison of F-bit and FEC framing in actual time.

	T_{RF}	99.9 %tile MRF	T_{OF}	99.9 %tile OFD	$T_{RF}+T_{OF}$	99.9 %tile RF+OF
F-bit	1.26 ms	1.6 ms	28 μs	133 μs	1.39 ms	1.73 ms
FEC	101 μs	212 μs	90.5 μs	164.4μs	191.5 μs	376.4 μs

The false in-frame times, T_{FF}'s, for FEC and F-bit framing for various values of c (reframe confirmation threshold) normalized to F-bit intervals (i.e. the value of c in the FEC case is multiplied by 8) are plotted in Fig. 5.1.

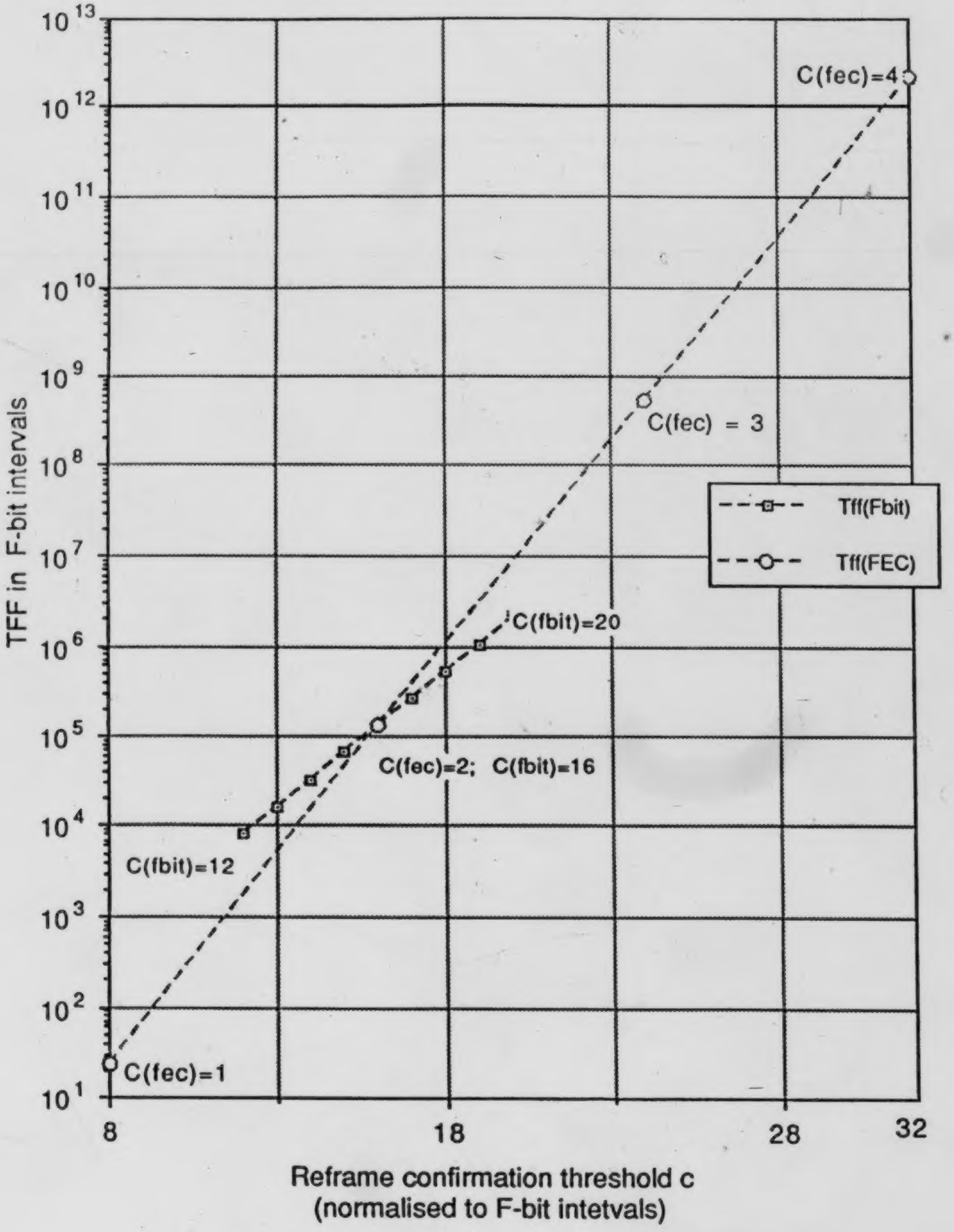


Fig. 5.1 Comparison of TFF's for F-bit and FEC Framing.

The T_{FF}'s (in units of F-bit interval) and the probabilities of a false in-frame declaration, P_F's, of the F-bit and FEC framing for the values of c selected in each case) are compared Table 5.4.

Table 5.4 Comparison of TFF's and PF's of the F-bit and FEC framing.

	T_{FF}	P_F
F-bit (c=20)	$2.1 * 10^{6}$	$1.61 * 10^{-4}$
FEC (c=3)	$5.38 * 10^{8}$	$1.99 * 10^{-8}$

As shown in Table 5.4, the false in-frame time of the FEC framing is 256 times longer than that for conventional F-bit framing. The chance of getting a false in-frame declaration has practically been eliminated in FEC framing.

The misframe times (in actual time) of the F-bit and various FEC OFD schemes are compared in Table 5.5 and Fig. 5.2.

Table 5.5. Comparison of the MF times for various OFD scheme in actual time.

Log(BER)	-4	-5	-6	-7	-8	-9
F-bit	7 days	19.4 yrs	$1.9 * 10^{4}$ yrs	$1.9 * 10^{7}$ yrs	$1.9 * 10^{10}$ yrs	$1.9 * 10^{13}$ yrs
FEC (c=6)	8 secs	1.8 mths	10^{6} yrs	$1.5 * 10^{11}$ yrs	$1.5 * 10^{16}$ yrs	$1.5 * 10^{22}$ yrs
SC (c=7)	9.1 secs	1.26 yrs	$4.5 * 10^{6}$ yrs	$9.1 * 10^{11}$ yrs	$1.7 * 10^{16}$ yrs	$1.7 * 10^{20}$ yrs
Hybrid (c=7)	9.5secs	1.2 yrs	$1.2 * 10^{6}$ yrs	$1.2 * 10^{10}$ yrs	$1.2 * 10^{14}$ yrs	$1.2 * 10^{18}$ yrs

The average times to a misframe, (T_{MF}) for FEC framing at degraded BER levels ($\leq 10^{-5}$) are not as long as those of F-bit framing. However the TMF's for the SC OFD and Hybrid OFD schemes at BER = 10^{-5} are longer than 1 year, and at BER levels lower than 10^{-6} for which FEC framing is recommended misframes practically never happen.

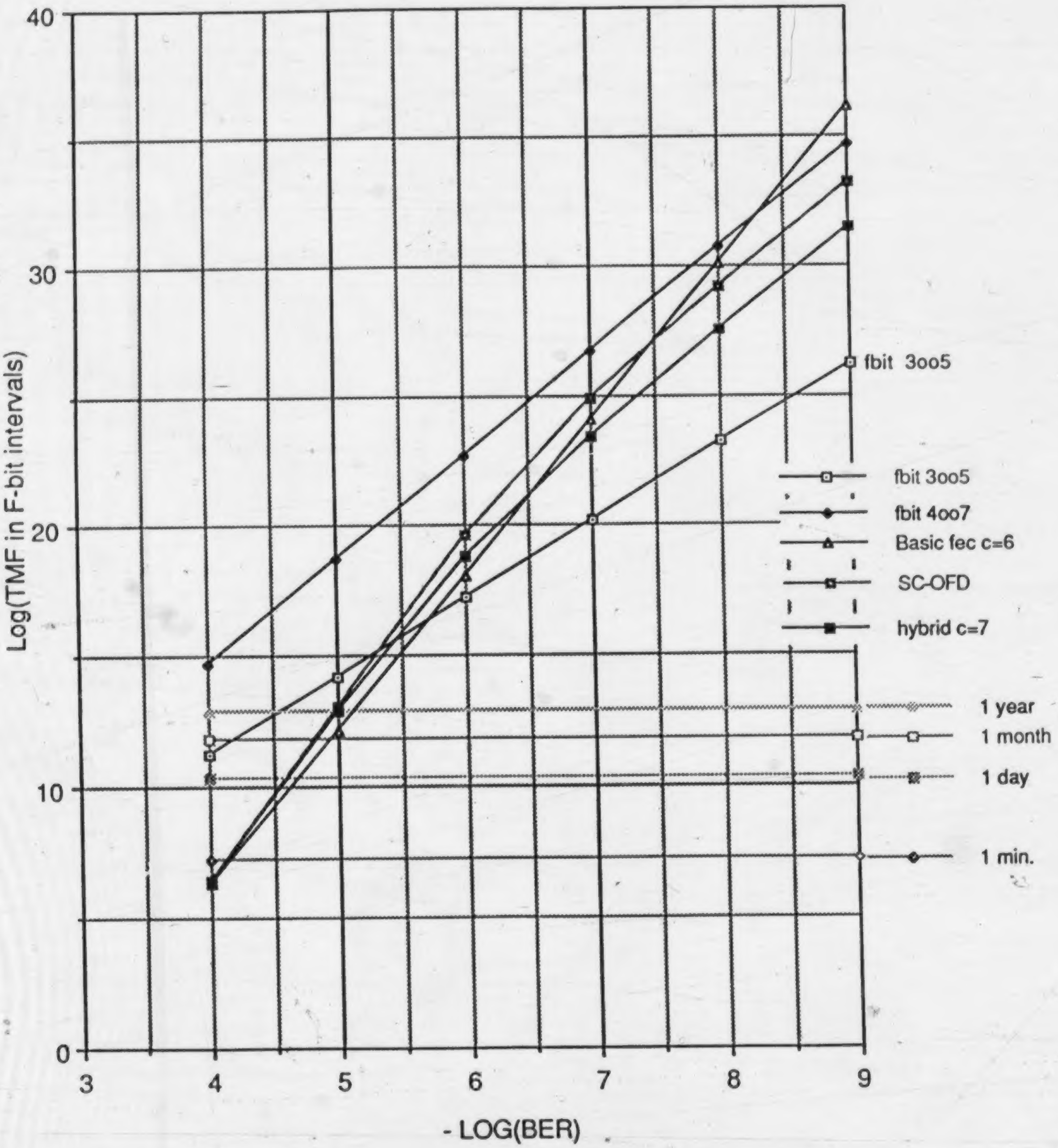


Fig. 5.2 Comparison of the TMF's for F-bit, Basic FEC, SC, and Hybrid OFD schemes.

6. COMBINED FRAMING AND FEC CODING FOR DS1

6.1 Selection of the FEC Code

The same concept of combined framing and FEC coding was applied to the DS1 signal format [1] where a Hamming code of (2316,2304) shortened from the parent code (4095,4083) was designed to span over 12 consecutive DS1 frames. The code has only SEC capabilities. The resulting FEC code word structure is as follows :

$$r_1[192]\ r_2[192]\ r_3[192]\ r_4[192]\ r_5\ [192]\ r_6\ [192]$$

$$r_7[192]\ r_8[192]\ r_9[192]\ r_{10}[192]\ r_{11}[192]\ r_{12}[192]$$

where r_1 to r_{12} are the parity check bit, protecting the entire block (they replace the primary framing F-bits) and [192] are the payload data bits.

The following irreducible polynomial was used as the generator polynomial [13]:

$$g(x) = x^{12} + x^6 + x^4 + x + 1 \tag{6.1}$$

The FEC encoding incurs a decoding delay of (2316/1.544Mbs) = 1.5 msec, which is acceptable for most voice and data applications. It has been estimated that the effective BER with the FEC protection is :

$$2981\ p_e^2 \tag{6.2}$$

where p_e is the raw BER, and the error events are assumed to be independent.

6.2 The CCSC for the FEC-DS1 Code

Repetition of the analysis in Subsec. 3.5.4. yields the relationship between syndromes $S_{i+1}(x)$ and $S_i(x)$ for the received words R_{i+1} and R_i (the systematic form of the block of bits in the receiver buffer at times i+1 and i) respectively, for the DS1 case:

$$S_{i+1}(x) = xS_i(x) \bmod g(x) + \mathrm{Ddistr}(x) \bmod g(x) \tag{6.3}$$

where

$$\mathrm{Ddistr}(x) = \sum_{j=1}^{25} d_j x^{p_j} \tag{6.4}$$

is the difference polynomial which accounts for the 25 differences between the left shift of R_i and R_{i+1}. d_j is the sum (modulo-2) of the appropriate pairs of bits in Rdistr_i (the block of bits in the receiver buffer at time i):

$$d_j = a_{j1} + a_{j2} \tag{6.5}$$

Note that j1 and j2 are bit positions in Rdistr_i.

The values of the position indices j1 and j2 (corresponding to a_{j1} and a_{j2} used to obtain d_j), and the associated values of p_j are given in Table 6.1.

Table 6.1 Values of j1, j2, and p_j for Ddistr(x).

d_j	d_1	d_2	d_3	d_4	d_5	d_6	d_7	d_8	d_9	d_{10}	d_{11}	d_{12}	d_{13}	d_{14}	d_{15}	d_{16}	d_{17}	d_{18}	d_{19}	d_{20}	d_{21}	d_{22}	d_{23}	d_{24}	d_{25}
j1	2315	2122	1929	1736	1543	1350	1157	964	771	578	385	192	2316	2123	1930	1737	1544	1351	1158	965	772	579	386	193	N/A
j2	N/A	2123	1930	1737	1544	1351	1158	965	772	579	386	193	0	2315	2122	1929	1736	1543	1350	1157	964	771	578	385	192
p_j	2316	2124	1932	1740	1548	1356	1164	972	780	588	396	204	12	11	10	9	8	7	6	5	4	3	2	1	0

Note that bit 2316 is the MSB of the receiver buffer at time i and bit 0 (used to compute d_{13}) is the newly arrived bit.

As before each of x^{p_j} mod g(x) is some fixed polynomial of degree less than n-k and can be precomputed and used in conjunction with d_j to obtain the syndrome $S_{i+1}(x)$ in a similar manner as described earlier. The syndromes for each of x^{p_j} mod g(x) in binary form are tabulated in Table 6.2.

Table 6.2 Syndromes [x^{p_j} mod g(x)] for $p_j \geq 12$.

d_j	p_j	syndrome (MSB first)
d_1	2316	100011011101
d_2	2124	011000000111
d_3	1932	101011011111
d_4	1740	011110011010
d_5	1548	110010001100
d_6	1356	110100101000
d_7	1164	111010100111
d_8	972	110001110001
d_9	780	010111100111
d_{10}	588	110100011011
d_{11}	396	100101010100
d_{12}	204	010000001010
d_{13}	12	000001010011

Note that the syndrome of each of x^{p_j} for $p_j < 12$ is equal to x^{p_j}.

The schematic architecture for realizing the CCSC scheme in the distributed case is shown in Fig. 6.1.

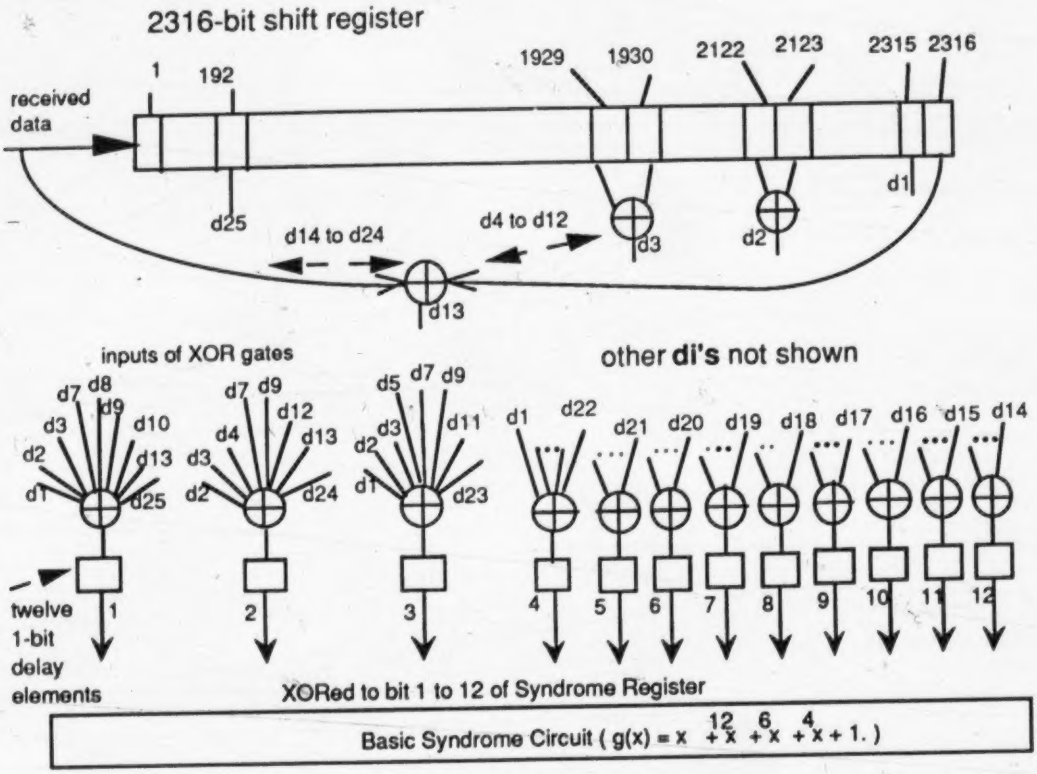

2316-bit shift register
received data
1
192
1929
1930
2122
2123
2315
2316
d1
d25
d14 to d24
d4 to d12
d3
d2
d13
inputs of XOR gates
other di's not shown
d1 d2 d3 d7 d8 d9 d10 d13 d25
d2 d3 d4 d7 d9 d12 d13 d24
d1 d2 d3 d5 d7 d9 d11 d23
d1 d22
d21 d20 d19 d18 d17 d16 d15 d14
twelve 1-bit delay elements
1 2 3 4 5 6 7 8 9 10 11 12
XORed to bit 1 to 12 of Syndrome Register
Basic Syndrome Circuit (g(x) = x^12 + x^6 + x^4 + x + 1.)

Fig. 6.1 CCSC circuit for the DS1-FEC code.

As before, the number of differing positions between R_i (or its left shift) and R_{i+1} is 25, which is greater than n-k =12. Therefore it can be shown that the probability of mimic, p_m, for the DS1-FEC code is always equal to 2^{-12} for all magnitudes of shift. Preliminary simulations have confirmed this theoretical result.

6.3 The Framing Performance of Conventional DS1 Framing

The specified value of the maximum average reframe time for the DS1 signal is 50msec [1]. A sequential search process, which meets this specification, and is capable of performing continuous slips during the search process is assumed.

The 3-o-o-5 OOF detection has been recommended and is analyzed here.

Using the analysis described in Chapter 2, the framing parameters expressed in units of DS1 F-bit intervals (193 bits) of conventional F-bit framing for the DS1 case are derived and tabulated in Table 6.3.

Table 6.3 Framing parameters for conventional DS1 framing.

	Mean	Standard Deviation	99.5 percentile	99.8 percentile	99.9 percentile
MRF[1]	405	19.68	458	465	470
FF[2]	$2.1 * 10^6$	$2.1 * 10^6$	N/A	N/A	N/A
OFD (3-o-o-5)	7.27	4.66	28	32	35

P_F (c=20, BER = 10^{-6}) = 0.00018308.

The values of T_{MF} (or their logarithms), in units of F-bit intervals for BER ranging from 10^{-4} to 10^{-10} are as follows:

Table 6.4 Misframe times for conventional DS1 framing.

Log(BER)	-4	-5	-6	-7	-8	-9	-10
Log(T_{MF}) (3-o-o-5)	11.2 (7.6 mths)	14.2 (628 yrs)	17.2	20.2	26.2	26.2	29.2

6.4 The Framing Performance of FEC Framing for DS1

Repeating the analysis done in Sec. 3.8, the framing parameters (in units of F-bit intervals) for the FEC framing for the DS1 case are analyzed and tabulated in Table 6.5.

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[1] The statistics of the RF time vary insignificantly as BER ranges from 10^{-6} to 10^{-11}.

[2] The standard deviation of the FF time is identical to that of its mean value.

Table 6.5 Framing parameters for DS1 FEC framing.

	Mean	Standard Deviation	99.5 percentile	99.8 percentile	99.9 percentile
MRF (c=2)	30.90	9.21	60	72	72
MRF[1] (c=3)	42.99	9.45	84	84	96
FF (c=2)	$1.36 * 10^5$	$1.36 * 10^5$	N/A	N/A	N/A
FF (c=3)	$5.57 * 10^8$	$5.57 * 10^8$	N/A	N/A	N/A
OFD(c=5)	60.04	1.39	60	60	72
OFD(c=6)	72.06	1.79	72	72	84

P_F (c=2,BER = 10^{-6}) = 1.39 * 10^{-4}, P_F (c=3,BER = 10^{-6}) = 3.39 * 10^{-8}; P_F's are obtained using (2.9).

The MRF and OF times obtained experimentally are tabulated in Table 6.6.

Table 6.6 Experimental framing parameters for DS1 FEC framing.

	Mean	Standard Deviation	99.5 percentile	99.8 percentile	99.9 percentile
MRF (c=3)	42.88	9.31	84	84	84
OFD (c=6)	72.06	1.59	72	72	96

The values of T_{MF} (or their logarithms), expressed in units of F-bit intervals, for BER ranging from 10^{-4} to 10^{-10} are shown in Table 6.7.

Table 6.7 Misframe times for DS1 FEC framing.

Log(BER)	-4	-5	-6	-7	-8	-9	-10
Log(T_{MF}) (c=5)	4.6 (5 secs)	9.3 (3 days)	14.3 (791 yrs)	19.3	24.3	34.3	39.3
Log(T_{MF}) (c=6)	5.28 (24 secs)	10.9 (4.1 mths)	16.9 (3.1 * 10^5 yrs)	22.9	28.9	34.9	40.9

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[1] The values for MRF (c=3) are for BER = 10^{-6}; for BER's ranging from 10^{-4} to 10^{-10}, the mean values range from 71.8 to 42.8 DS1 F-bit intervals.

6.5 Selection of the Reframe and Out-of-frame Detection Confirmation Threshold

The reframe confirmation threshold c has been chosen as 3 because values lower than 3 do not give long enough T_{FF} (and small enough value of P_F). The OOF detection confirmation threshold has been chosen as 6 because values lower than 6 would not guarantee long enough T_{MF} for degraded BER (such as 10^{-5}). At usual BER's of below 10^{-8}, misframes practically never happen.

6.6 Comparison of FEC and F-bit Framing for DS1

The MRF, OFD, and the combined MRF and OFD times (in units of F-bit intervals) , for the selected values of the confirmation threshold, for the F-bit and FEC framing are compared in Table 6.8.

Table 6.8 Comparison of F-bit and FEC framing in units of F-bit intervals.

	T_{RF}	99.9 percentile MRF	T_{OF}	99.9 percentile OFD	$T_{RF}+T_{OF}$	99.9 percentile MRF+OFD
F-bit	409	470	7.27	35	416.27	477.27
FEC	42.99	96	72.06	84	115.05	180

As shown in Table 6.8, the maximum average reframe time with FEC framing is 9.5 times less than with conventional F-bit framing. Although the T_{OF} of FEC framing is almost 10 times as long as that of F-bit framing, its 99.9 percentile value is only 2.5 times that of F-bit framing. Because an OOF detection is always followed by a reframe, it is logical to consider their combined value. The combined value of T_{OF} and T_{RF} for FEC framing (i.e. the duration of time between a loss of alignment and subsequent re-alignment) is nearly one quarter that for F-bit framing. The combined 99.9 percentile value is roughly fourty percent of that for F-bit framing.

7. CONCLUSIONS

7.1 Summary and Conclusions

The combined framing and FEC coding scheme has been successfully applied to the DS3 (and DS1, in Chapter 6) signal format by replacing (reusing) F and C bits with FEC check bits (without altering the bit rate or the masterframe structure of the DS3 signal).

The framing performance of conventional F-bit framing has been analyzed to establish a benchmark against which that of FEC framing can be compared.

The initial problem of slow reframing speed (for FEC framing) due to the way that a normal decoder computes a syndrome (reset and restart) was overcome by the development of the novel continuously compensated syndrome computation (CCSC) scheme for the DS3-FEC (and DS1-FEC) codes. When developing the specific CCSC scheme for the DS3-FEC code, the general (applicable to any code word length) CCSC schemes for other code word formats including the systematic, shortened and extended systematic, and the systematic reversed formats were also developed. The probability of mimic for each considered case was also analyzed and experimentally determined. The theoretical and experimental results showed remarkable agreement. It was found that the reframing times of the distributed (DS3-FEC) and the systematic reversed codes are the shortest because they have the lowest probability of mimic.

The framing performance of FEC framing was analyzed. It was found to be better than that of conventional F-bit framing. From the analyzed results, the optimal reframing and OFD confirmation criteria were determined. A second problem arose when it was found that the OFD times of FEC framing are not as good (short) as those of F-bit framing. To improve the OFD times, the Shortened Code (SC) OFD and Hybrid OFD schemes for the DS3 case, which use additional information available in the triple error detection process and the masterframe overhead, were developed.

The OFD times for these two schemes (especially the Hybrid OFD scheme) were significantly improved and become comparable to those of F-bit framing.

All the reframe and OOF detection performance parameter values were experimentally verified using computer simulations, and the experimental results were remarkably consistent with the theoretical ones.

The gain in framing performance achieved with the FEC framing for the DS3 case can be summarized as follows:

- Reframing Speed - 13 times faster.
- OOF detection Speed - 3.3 times slower (note: not as good).
- OFD + Reframe time - 7 times shorter.
- Chance of a false in-frame - practically eliminated in FEC framing.
- Misframe - about once a year at BER = 10^{-5}, and practically never happen at lower BER's.

The gain in BER performance of the proposed DS3-FEC scheme was analyzed. It was found that the application of FEC reduces the payload BER to about 1360 $(BER_{channel})^2$.

To study the effect of the scheme on a real commercial DS3 circuit, a 22 days log of continuous error-second data for a commercial circuit was obtained. The data showed that errors occurred mostly in isolation (in 97% of all cases), and it was also determined that the single error correcting FEC code would have corrected almost all the errors during the logged period; the overall BER would have been reduced from 1.4×10^{-11} (the average BER of this circuit) to 7.6×10^{-18}.

The proposed scheme was also applied to the DS1 signal format (as an example). The CCSC circuit and the resulting framing and BER performances involved were analyzed and presented. It was also found that similar (although to a lesser extent) gain in framing and BER performances was achieved when applying the scheme to the DS1 signal format.

7.2 Further Work

The various CCSC schemes developed in this thesis enable fast framing using only the FEC information. It is envisaged, by employing the appropriate CCSC, the combined framing and FEC concept can also be applied to signal formats other than discussed here (e.g. CEPT formats [14]).

A preliminary estimate for the VLSI implementation of the proposed combined framing and FEC scheme for the DS3 signal format indicates that a 1360 bit shift register and fewer than 3000 gates are required. Various aspects regarding the implementation of the framing and error control circuitry for the proposed scheme have been depicted using schematic architectures in Chapter 3. Further design work and prototyping are required before implementing the combined framing and FEC coding scheme in commercial DS3 circuits.

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APPENDIX A

This appendix discusses how to obtain the probability generating function (PGF), $P_X(z)$, of a given random variable X, from its state transition probability matrix. The PGF is of interest because, once the PGF has been obtained, other statistics can also be obtained easily as described in Subsec. 2.4.1.

Discrete Markov processes (or Markov chains) are customarily described by the difference equations which indicate how the probability of being in the state at time $t = n+1$ depends on the probabilities of being in adjacent states at $t = n$. In general the probability of being in state k at time n+1 is given by:

$$p_k(n+1) = \sum_{j=1}^{M} p_{jk}\, p_j(n) \qquad \text{(A.1)}$$

where M is the total number of states, and p_{jk} is the transition probability from state j to state k. An equation equivalent to (A.1) can be written for each of the states from 1 to M.

The resulting set of difference equations can be represented in matrix form:

$$[p1(n+1), p2(n+1), \dots, pM(n+1)] = [p1(n), p2(n), \dots, pM(n)] \begin{bmatrix} p_{11} & \cdots & p_{1M} \\ \vdots & & \vdots \\ p_{M1} & \cdots & p_{MM} \end{bmatrix} \qquad \text{(A.2)}$$

Eqn. (A.2) can be rewritten as:

$$\underline{p(n+1)} = \underline{p(n)}\, \underline{Q} \qquad \text{(A.3)}$$

where $\underline{p(n+1)}$ and $\underline{p(n)}$ are the row matrices of state probabilities at time n+1 and n respectively, and $\underline{Q}$ is the state transition probability matrix (previously used in Chapter 2 and 4 to determine the OFD and MF times).

Given the initial value $\underline{p(0)}$ the matrices $\underline{p(n)}$ can be determined from (A.3) as follows:

$$\underline{p(1)} = \underline{p(0)}\,\underline{Q}$$

$$\underline{p(2)} = \underline{p(0)}\,\underline{Q}^2$$

$$\underline{p(3)} = \underline{p(0)}\,\underline{Q}^3$$

$$\vdots$$

and in general:

$$\underline{p(n)} = \underline{p(0)}\,\underline{Q}^n;\ n \geq 0 \tag{A.4}$$

where $\underline{Q}^0 = I$, the identity matrix.

To obtain the PGF, $\underline{P(z)}$, we proceed to the transform domain. The z-transform $\underline{Q(z)}$ of the matrix sequence $\underline{Q}^n$, n = 0, 1, 2, ..., is in a way analogous to that used when taking the z-transform for a sequence of numbers. We define,

$$\underline{Q(z)} = \sum_{n=0}^{\infty} z^n\,\underline{Q}^n \tag{A.5}$$

$\underline{Q(z)}$ is defined as a matrix series convergent near the point $z = 0$.

$\underline{P(z)}$ is defined as the matrix z-transform of $\underline{p(n)}$:

$$\underline{P(z)} = \sum_{n=0}^{\infty} z^n\,\underline{p(n)} \tag{A.6}$$

Transforming both sides of (A.4), we obtain

$$\underline{P(z)} = \underline{p(0)}\,\underline{Q(z)} \tag{A.7}$$

To evaluate $\underline{Q(z)}$ we left multiply (A.5), its defining equation, by the matrix $\underline{R} = (I - z\underline{Q})$ as follows:

$$\begin{aligned}(I - z\underline{Q})\,\underline{Q(z)} &= (I - z\underline{Q}) \sum_{n=0}^{\infty} z^n \underline{Q}^n \\ &= \sum_{n=0}^{\infty} z^n \underline{Q}^n - \sum_{n=0}^{\infty} z^{n+1} \underline{Q}^{n+1} \\ &= I \end{aligned} \tag{A.8}$$

Hence,

$$\underline{Q(z)} = (I - z\underline{Q})^{-1} = \underline{R}^{-1} \tag{A.9}$$

where $(I - z\underline{Q})^{-1}$ is the inverse of $(I - z\underline{Q})$. Therefore, substituting (A.9) into (A.7), we get:

$$\underline{P(z)} = \underline{p(0)}\,(I - z\underline{Q})^{-1} \tag{A.10}$$

In general each element $P_i(z)$ of $\underline{P(z)}$ is the PGF for the transfer from the initial state defined in $\underline{p(0)}$ to the state i. In our problem, the PGF of interest is for the transfer from the in-frame state (or state 1) to the out-of-frame state (or the final state M). If we substitute $\underline{p(0)} = [1, 0, 0, \ldots, 0]$, and $P_M(z)$ becomes the PGF for the OFD (or MF) time. Therefore, by substiting $\underline{p(0)} = [1, 0, 0, \ldots, 0]$ into (A.10) we obtain the last element (or the Mth column) of $\underline{P(z)}$ as follows:

$$P_M(z) = [1, 0, 0, \ldots, 0]\,(I - zQ)^{-1} \begin{bmatrix} 0 \\ 0 \\ \cdot \\ \cdot \\ 1 \end{bmatrix} \tag{A.11}$$

Now the right hand side of (A.11) reduces to v_{1M}, the element in the 1st row and Mth column of $(I - z\underline{Q})^{-1} = R^{-1}$. From matrix algebra we know that

$$v_{1M} = \frac{R_{M1}}{|R|} \qquad \text{(A.12)}$$

where R_{M1} is the cofactor of the element r_{M1}, and $|R|$ is the determinant of the matrix $\underline{R}$. Finally, by combining (A.11) and (A.12) we obtain,

$$P_M(z) = \frac{R_{M1}}{|I - z\,Q|} \qquad \text{(A.13)}$$

APPENDIX B

The weight distribution of a Hamming code of length n is defined as follows [12]:

The number of code vectors of weight i, V_i, is simply the coefficient of z^i in the expansion of the following polynomial:

$$V(z) = \frac{1}{n+1}\{(1+z)^n + n(1-z)(1-z^2)^{(n-1)/2}\} \tag{B.1}$$

This polynomial is the weight enumerator for the Hamming codes. However, for extended Hamming codes, used in the DS3-FEC code, the weight distribution is defined as follows [12].

The number of code vectors of weight i, W_i, is the coefficient of z^i in the expansion of the following polynomial:

$$W(z) = 1/2[V(z) + V(-z)] \tag{B.2}$$

Combining (B.1) and (B.2) we obtain,

$$W(z) = \frac{1}{2(n+1)}\frac{1}{n+1}\{(1+z)^n + (1-z)^n + 2n(1-z^2)^{(n-1)/2}\} \tag{B.3}$$

APPENDIX C

A BER ANALYSIS OF A COMMERCIAL DS3 CHANNEL

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24 May 1989

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25 May 1989

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26 May 1989

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4 June 1989

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5 June 1989

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6 June 1989

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7 June 1989

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9 June 1989

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10 June 1989

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11 June 1989

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12 June 1989

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13 June 1989

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14 June 1989
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Legend :
- : an error free 60 seconds interval.
1-9 : 1 to 9 single errored second(s) in the 60 seconds interval
a : 10 single errored seconds in the 60 seconds interval.
b : 11 single errored seconds in the 60 seconds interval.
c : 12 single errored seconds in the 60 seconds interval.
d : 13 single errored seconds in the 60 seconds interval.
P : A Double (Paired) errored second in the 60 seconds interval.
T : A Triple errored second in the 60 seconds interval.

Total elapsed minutes in this error events study is : 31006
Total number of errors for the above duration is : 1189

The number of Double Errored seconds is : 15
The number of Triple Errored seconds is : 1

The RAW BER of the monitored data is : 1.4E-11
Assuming a SEC-DED code has been used to protect the above data then the Effective BER(s) are listed as follows :

If only errors occurring in single errored seconds are corrected, then :
The EFFECTIVE BER is : 4.1E-13

If most* of the errors occurring in all double(or triple) errored seconds are also corrected, then :
The EFFECTIVE BER becomes : 7.67 E-18

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* i.e. assuming errors occurring in double (or triple) errored seconds are independently distributed within the 1 second interval.